## Student Activity

How long (in ns) does each instruction take?

|  | Single <br> Cycle | Multi- <br> cycle | Which ones are <br> faster in <br> Multi-cycle? |
| :--- | :--- | :--- | :--- |
| loads |  |  |  |
| stores |  |  |  |
| branches |  |  |  |
| arithmetic |  |  |  |
| Cycle Time |  |  |  |


| Student Activity |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| How long does it take to execute a sequence of four lw instructions? |  |  |  |  |  |
|  | Instruction Fetch | Register Read | ALU Operation | Data Access | Register Write |
| Load Word (lw) | 200 ps | 100 ps | 200 ps | 200 ps | 100 ps |

Iw \$1, 100 (\$0)
Iw \$1, 104 (\$0)
Iw \$1, 108 (\$0)
Iw \$1, 112(\$0)

Single Cycle $=\square$
(Time in ps)


## Student Activity

## Reading Pipeline Diagrams

|  |  | Clock cycle |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| Iw | \$t0, 4(\$sp) | IF | ID | EX | MEM | WB |  |  |  |  |
| sub | \$v0, \$a0, \$a1 |  | IF | ID | EX | MEM | WB |  |  |  |
| and | \$t1, \$t2, \$t3 |  |  | IF | ID | EX | MEM | WB |  |  |
| or | \$s0, \$s1, \$s2 |  |  |  | IF | ID | EX | MEM | WB |  |
| add | \$sp, \$sp, -4 |  |  |  |  | IF | ID | EX | MEM | WB |

1. What cycle is the "add" instruction being fetched in? $\square$
2. What is the last cycle where the "or" instruction is active? $\square$
3. What happens in cycle 4?
