CSE 378, 06wi – Lecture 3 Main Points
Introduction to the MIPS ISA

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Operands in memory

- "unit of addressing" is the byte
- opcode determines "unit of transfer:
  - e.g., LW (4-bytes) / LH (2-bytes) / LB (1-byte)
- base-offset addressing
  - LW $8, 12($5) # load 4 bytes at address ($5)+12 into $8
  - LB $8, 7($5) # load 1 byte (sign-extended) at ($5)+7 into $8
- operands must be "aligned"

Logical Operations

- and, or, xor, nor (andi, ori, xori)
- and masks / or masks
- shifts:
  - sll, srl: immediate shift amount, zero filled
  - sra: immediate shift amount, sign-extended
  - srlv, sllv, srav: shift amount is in a register

Branching

- Can be thought of as an assignment to the PC
- Conditional branching:
  - beq, bne: compare two registers
  - bgez, bltz: compare a register to 0
  - slt/slti: "set on less than (immediate)" Result is 0 (false) or 1 (true)
- Unconditional branching:
  - j, jr: new pc value is in the instruction (j) or in a register (jr)

Compiling

- Going from a high-level language representation of a program to an equivalent sequence of assembler instructions