

Configuration Information

- Discuss caches with properties ...
 - 32-bit addresses
 - 16-byte lines
 - 256-byte capacity
 - Memory references are either Read/Write

Schematic Cache

0:				
1:				
2:				
3:				
4:				
5:				
6:				
7:				
8:				
9:				
A:				
B:				
C:				
D:				
E:				
F:				

Schematic 2-Way Cache

0:							
1:							
2:							
3:							
4:							
5:							
6:							
7:							

Generic Line

d 000000																			
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Traces—Instructions 1

```
0xAA10 R
0xAA14 R
0xAA18 R
0xAA1C R
0xAA20 R
0xAA24 R
0xAA28 R
0xAA2C R
0xAA30 R
0xAA34 R
0xAA1C R
0xAA20 R
0xAA24 R
...
```

Traces 2 (Conflicts)

```
0xAA10 R
0xAA14 R
0xAA18 R
0xAA1C R
0xBC60 R
0xAA20 R
0xAA24 R
0xDD40 R
0xFF90 R
0xAA28 R
0xAA2C R
0xAA30 R
0xCB68 R
```

Traces 3 (Conflicts)

0xAA34 R
0xAA1C R
0xBC64 R
0xAA20 R
0xAA24 R
0xDD44 R
0xFF90 R
0xAA28 R
0xAA2C R
0xAA30 R
0xCB6C R
...

Traces 4 (Conflicts)

0xAA34 R
0xAA1C R
0xBC68 R
0xAA20 R
0xAA24 R
0xDD48 R
0xFF90 R
0xAA28 R
0xAA2C R
0xAA30 R
0xCB70 R

Traces 5 (Conflicts)

0xAA1C R
0xBC6A R
0xAA20 R
0xAA24 R
0xDD4C R
0xFF94 R
0xAA28 R
0xAA2C R
0xAA30 R
0xCB74 R
...

Traces 6 (Conflicts, Writes)

0xAA10 R
0xAA14 R
0xAA18 R
0xAA1C R
0xBC10 W
0xAA20 R
0xAA24 W
0xDD40 R
0xFF90 R
0xCC28 W
0xAA2C R
0xAA30 R
0xCB18 W
...

Traces 7 (Conflicts, Writes)

0xAA24 R
0xAA1C R
0xBC68 W
0xAA20 R
0xAA24 W
0xDD48 R
0xFF90 R
0xCC28 R
0xAA2C R
0xAA30 R
0xCB70 R
...

Traces 8 (Conflicts, Writes)

0xAA24 R
0xAA1C R
0xBC64 W
0xAA20 R
0xAA24 W
0xDD44 R
0xFF90 R
0xCC28 R
0xAA2C R
0xAA30 R
0xCB6C W
...

Direct Mapped Cache

0:		
1:		
2:		
3:		
4:		
5:		
6:		
7:		
8:		
9:		
A:		
B:		
C:		
D:		
E:		
F:		

Direct Mapped Cache WB

0:			
1:			
2:			
3:			
4:			
5:			
6:			
7:			
8:			
9:			
A:			
B:			
C:			
D:			
E:			
F:			

2-Way Set Associative Cache

		:0:			
		:1:			
		:2:			
		:3:			
		:4:			
		:5:			
		:6:			
		:7:			

2-Way Set Associative Cache WB

				:0:			
				:1:			
				:2:			
				:3:			
				:4:			
				:5:			
				:6:			
				:7:			