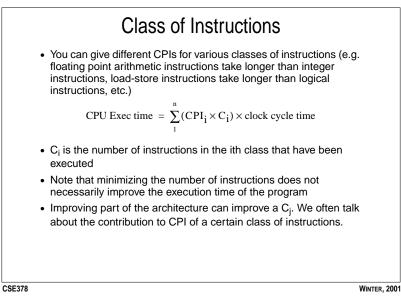
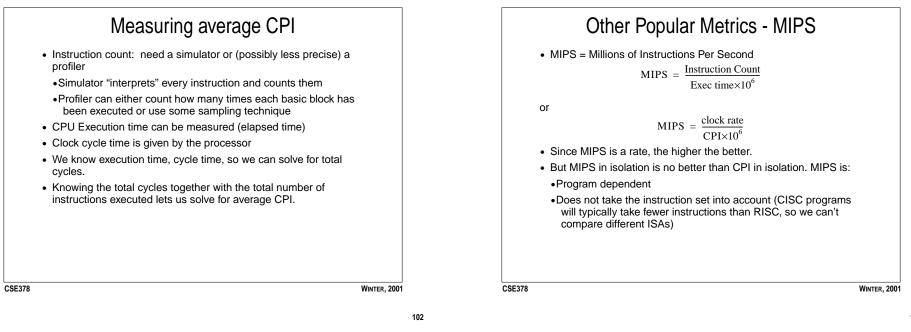
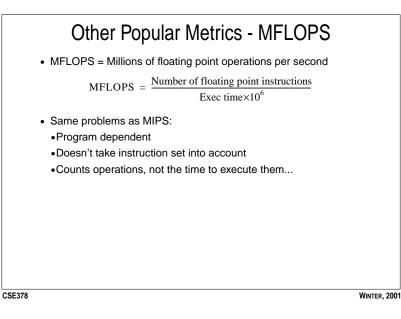


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The Trouble with MIPS

•Machine A with compiler C1 executes program P in 10 seconds,

•Machine A with compiler C2 executes program P in 15 seconds,

• While C1 is clearly faster than C2, C1 has a lower MIPS rating

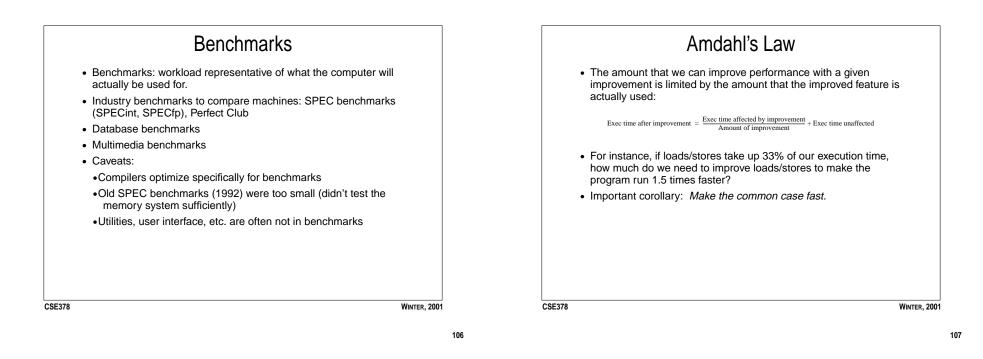
• ... the trouble with MIPS is that it doesn't take CPI into account.

• Using MIPS can give "wrong" results:

than C2....

using 100,000,000 instructions (10 MIPS)

using 180,000,000 instructions (12 MIPS)

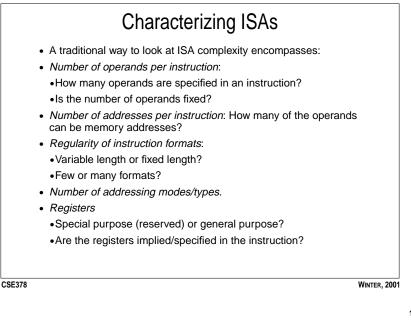


Instruction Category	GCC	SPICE	Ave. CPI
Load/Store	33%	40%	1.4
Branch	16%	8%	1.8
Jumps	2%	2%	1.2
FP Add	-	5%	2.0
FP Sub	-	3%	4.0
FP Mul	-	6%	5.0
FP Div	-	3%	19.0
Other (Integer add/sub, stl, etc)	49%	33%	1.0

CPI for a given category to be the same btwn two programs?

Evolution of ISAs

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A Tour of Common Addressing Modes

Name	Example	Meaning
* Immediate	100	100
* Register	r6	Contents of r6
Register Deferred	(r6)	Memory[r6]
* Based/Displacement	100(r6)	Memory[r6+100]
* PC-Relative	100	PC + 100
Deferred	@100(r6)	Memory[Memory[r6+100]]
Autoincrement	(r3)+	Memory[r3]; r3 = r3 + size
Autodecrement	-(r3)	r3 = r3 - size; Memory[r3]
Autoincrement deferred	@(r3)+	Memory[Memory[r3]]; r3 = r3 + size

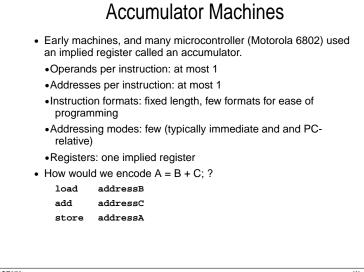
· We use VAX-like asm notation for non-MIPS addr modes...

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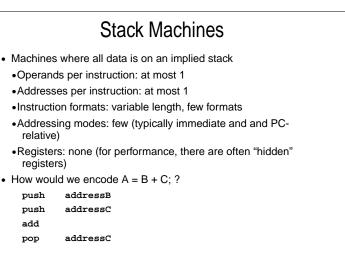
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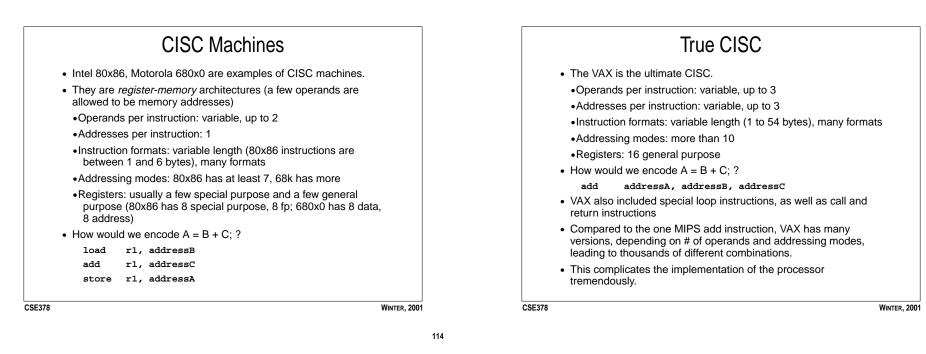


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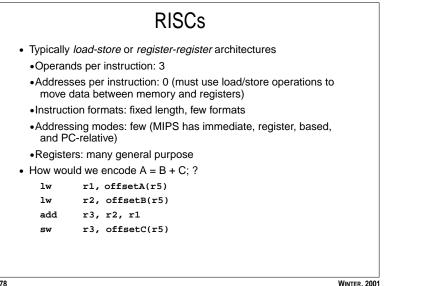


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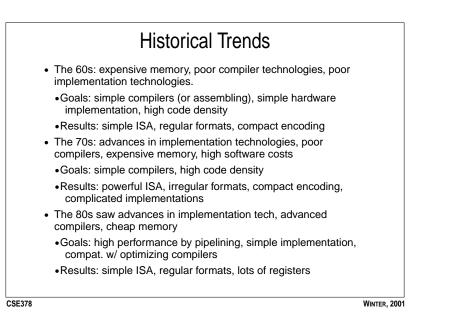




Summary Comparisons

	Accumulator	Stack	CISC	RISC
Implementation	easy	easy	hard	easy
Instruction density	high	high	high	low
Assembly coding	easy	medium	easiest	tiresome
Compilation	easy	easy	easy	hard
Memory overhead	high	high	highest?	lower
Instruction count	medium	medium	low	high
СРІ	medium	medium	high	low
Cycle time	?	?	high	low

• If RISCs have high instruction count, how can they possibly achieve such good performance?



Some Modern Processors

Processor	Mhz	Year	Style	Trans. x 10 ⁶	SpecInt/Fp92	SpecInt/Fp95
Intel 386DX	33	1987	CISC	0.275	8/3	
R3000	40	1988	RISC	0.3	28/36	
Motorola 68040	25	1989	CISC	1.2	21/15	
Intel 80486DX	50	1991	CISC	1.2	33/15	
R4400	250	1995	RISC	2.2	180/180	
Intel P6	166	1996	CISC	5.5	~290/260	~7/6
Dec Alpha 21164	300	1995	RISC	9.3	~330/500	~9/13
Intel PIII	1000	2000	CISC	28	~1800/1800	~45/45
SPARC Ultra III	900	2000	RISC	28	~2000/3000	~50/90

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