

CSE378 Practice Cache Problems

**Problem 1.**

Given a 2 way set associative cache with 2 word blocks and a total size of 32 words, show the final state of the cache after the following address stream from the processor occurs.

00000080  
 00000084  
 00000088  
 00000144  
 00000148  
 0000014C  
 00000150  
 00000160  
 00000080  
 00000084  
 00000088  
 0000008C  
 00000090

Assume that all requests are reads and that the cache is initially empty. Assume LRU replacement policy.

Calculate how many cycles are required to complete this address stream, if cache hit time is 1 cycle, and miss penalty is  $10 + W$  cycles, where  $W$  is the cache width. (So it takes 11 cycles to read/write the first word, and 1 cycle to read/write the next one).

Show the final state of the cache in the following table:

Line #	set 0					set 1				
	tag	data0	data1	valid	lru	tag	data0	data1	valid	lru
0										
1										
2										
3										
4										
5										
6										
7										

**Problem 2.**

Using the series of references given in Problem 1, show the final state of of the cache for a direct-mapped cache with 8 word blocks and a total size of 32 words. Also calculate the number of cycles required for the address stream, if cache hit time is 1 cycle, and miss penalty is  $10 + W$  cycles, where  $W$  is the cache width.

**Problem 3.**

To reduce conflict misses, you decide to add a small, 1 entry victim buffer (holds one cache line) to the direct-mapped cache from problem 2. Show the final state of the cache and the victim buffer after the address stream given in problem 1 executes.

Calculate how many cycles are required to complete this address stream, if cache hit time is 1 cycle, victim buffer hit time is 2 cycles, and miss penalty is  $10 + W$  cycles, where  $W$  is the cache width.

**Problem 4.**

Given a 2 way set associative cache with 2 word blocks and a total size of 32 words, show the final state of the cache after the following address stream from the processor occurs.

OFF00F70 (R)  
 OFF00F60 (W)  
 OFE0012C (R)  
 OFF00F5C (R)  
 OFE0012C (W)  
 OFE001E8 (R)  
 OF000F64 (R)  
 OF000144 (R)  
 OFE00204 (W)  
 OFF00F74 (W)  
 OF000F64 (R)  
 OFE00EF4 (R)  
 OF000BB4 (R)

Assume LRU replacement policy. Assume write-back, write-allocate policy.

Calculate how many cycles are required to complete this address stream, if cache hit time is 1 cycle, and miss penalty is  $10 + W$  cycles, where  $W$  is the cache width.

Show the final state of the cache in the following table:

Line #	set 0						set 1					
	tag	data0	data1	valid	lru	dirty	tag	data0	data1	valid	lru	dirty
0												
1												
2												
3												
4												
5												
6												
7												

**Problem 5.**

Now assume the cache from problem 4 is write-through, and write-around (no allocate on write). Calculate the final state of the cache and number of cycles for the address stream.

**Problem 6.**

Repeat problems 4 and 5 for a direct-mapped cache with 4 word blocks and a total cache size of 32 words.

**Problem 7.**

You have a machine configured as follows:

42-bit virtual address

32-bit physical address

32Kb, 2-way set associative cache with 16-word blocks

32-entry TLB (fully associative)

3-level page table (top level has 256 entries, next levels have 1024 entries).

Assume that, as you've previously seen, the VPN in this machine is the same as the cache tag and that the lower bits of the address are concatenated with the PFN to form the physical address.

How big is the Virtual Page Number (VPN)?

How big is the Page Frame Number (PFN)?

How big is the cache tag?

Which bits of the VPN are used for accessing the top-level page table?

Which bits of the VPN are used for accessing the second-level page table?

Which bits of the VPN are used for accessing the third-level page table?

**Problem 8.**

Using the information in the page tables on the following page, translate the sequence of virtual addresses on the last page (labeled "R"ead or "W"rite) to physical addresses, show the final contents of the TLB and cache, calculate the TLB and cache hit ratios, and update page table bits if necessary. Which references cause page faults? Write protection errors? Note that the virtual address is only 11 bits while the physical address is 16 bits. The machine configuration is a 4-entry, fully associative TLB, a 2-way set associative cache with 4-word blocks and 32 words total, and a 2-level paging mechanism with 4 entries in the top level and 8 entries at the next level.

The TLB:

TLB Entry	VPN	PFN	valid	dirty	prot	LRU
0						
1						
2						
3						

The cache:

Line #	set 0					set 1				
	tag	data0-3	valid	lru	dirty	tag	data0-3	valid	lru	dirty
0		X					X			
1		X					X			
2		X					X			
3		X					X			

Table 0x0:

PFN	V	D	P
0x110	0	0	1
0x100	0	0	1

Table 0x1:

PFN	V	D	P
0x220	0	0	0

Top levelpage table:

0x0
0x1
0x2
0x3

Table 0x2:

PFN	V	D	P
0x200	0	0	1

Table 0x3:

PFN	V	D	P

Virtual Addresses:

0x040 (R)  
0x044 (R)  
0x048 (R)  
0x020 (R)  
0x200 (R)  
0x024 (R)  
0x204 (R)  
0x028 (R)  
0x208 (W)  
0x02c (R)  
0x020 (R)  
0x208 (R)  
0x024 (R)  
0x20c (R)  
0x028 (R)  
0x210 (W)  
0x02c (R)  
0x020 (R)  
0x210 (R)  
0x024 (R)  
0x214 (R)  
0x028 (R)  
0x218 (W)  
0x04c (R)  
0x418 (W)  
0x050 (R)  
0x000 (R)