University of Washington – College of Engineering
Spring 2026 Instructor: Justin Hsia 2026-05-28

EE/CSE 371 QUIZ 5

Name: ______________________________

Student ID Number: ________________

Please do not turn the page until 11:30.

Instructions

- This quiz contains 4 pages, including this cover page. You may use the backs of the pages for scratch work.
- The quiz is closed book and closed notes, though scientific calculators are allowed.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all headphones and watches.
- You have 50 minutes to complete this quiz.

Advice

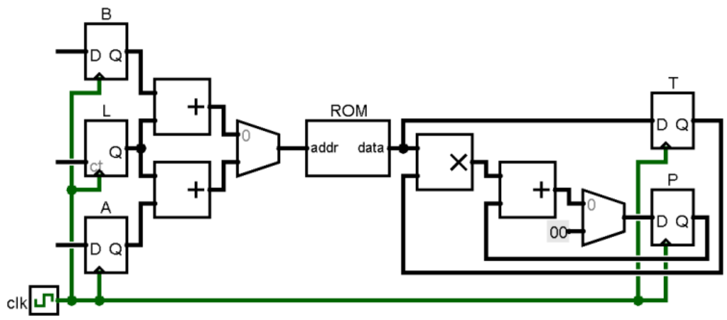
- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax.

Static Timing Analysis [10 pts]

setup slack = $DRT_{su} - DAT_{su}$ = min clock path – max data path
hold slack = $DAT_h - DRT_h$ = min data path – max clock path

We will analyze the dot product algorithm datapath from Quiz 4 with the given timing constants.

- Assume t_{su}, t_h, and t_{CO} are the same for all registers, including counter L.
- Notice that this circuit has paths with feedback!



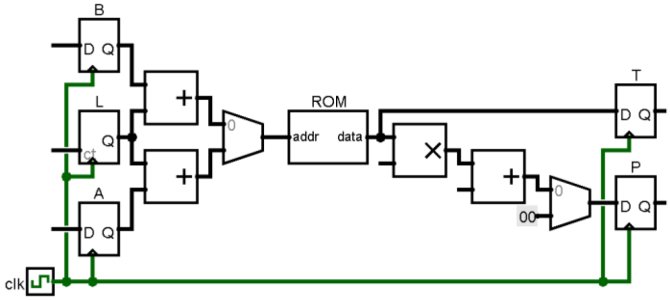
$T = 175$ ns,	$t_{su} = 17$ ns
$t_{wire} = 0$,	$t_h = 8$ ns
$t_{clkB} \in [4, 7]$ ns,	$t_{CO} \in [9, 12]$ ns
$t_{clkL} \in [2, 5]$ ns,	$t_+ \in [20, 25]$ ns
$t_{clkA} \in [1, 4]$ ns,	$t_\times \in [43, 50]$ ns
$t_{clkT} \in [3, 7]$ ns,	$t_{MUX} \in [11, 15]$ ns
$t_{clkP} \in [2, 6]$ ns,	$t_{ROM} \in [16, 19]$ ns

Solve for the setup slack and hold slack for this circuit, and put your answers in the boxes below. You are allowed to use a calculator on this problem, but no credit will be given without work.

Setup Slack:	ns
Hold Slack:	ns

Pipelining [12 pts]

We will look at a simplified version of the same circuit (*i.e.*, we will ignore/omit the feedback):



$t_{su} = t_h = t_{wire} = t_{clk} = 0$

$t_{CO} = 12$ ns (all regs)

$t_+ = 25$ ns, $t_\times = 50$ ns

$t_{MUX} = 15$ ns, $t_{ROM} = 19$ ns

1) **Complete *both copies* of the Data Flow Graph (DFG) for the circuit** by adding nodes labeled with their delays and edges. Note that B, L, A, T, and P correspond to the outputs of those registers. One node, corresponding to the top-left [+] gate, has been provided for you.

2) **Draw cutsets on your two DFGs to make a 2-stage pipelined and a 3-stage pipelined version of this circuit with *minimal clock period*.** The signals T and P should remain in sync.

3) Assuming we use the minimum clock periods, **compute the latency** for both pipelined versions of this circuit and write them into the boxes below. No credit will be given without work.

2-stage pipeline:

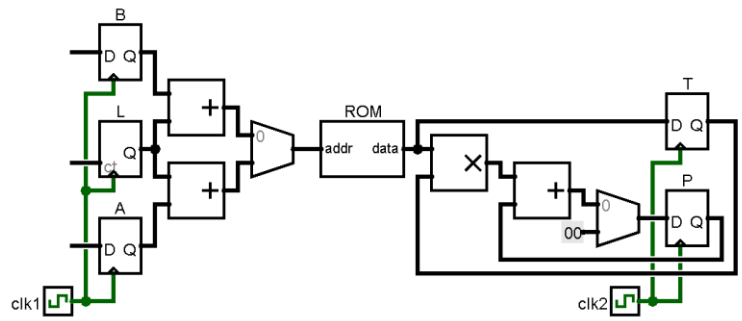
Latency: ____ ns

3-stage pipeline:

Latency: ____ ns

Clock Domain Crossing [4 pts]

We tweaked the circuit so that registers T and P are now controlled by a separate clock with unknown relationship between clk1 and clk2:



a) A good practice we discussed was to make sure that all clock domain crossings are registered to reduce the frequency of input changes. To implement this practice, **how many registers do we need to add** to the circuit shown above? **Where do we need to place them**?

b) Another good practice we discussed was to have a 2-flip flop synchronizer after every clock domain crossing. To implement this practice, **how many registers do we need to add** to the circuit shown above (*i.e.*, ignore part A)? **Where do we need to place them**? Be sure to describe which clock each register is connected to (clk1 or clk2).

[End of Quiz]