University of Washington – College of Engineering

Spring 2024 Instructor: Justin Hsia 2024-05-23

EE/CSE371 QUIZ 5

Name: _____

Student ID Number: _____

Please do not turn the page until 11:30.

Instructions

- This quiz contains 4 pages, including this cover page. You may use the backs of the pages for scratch work.
- The quiz is closed book and closed notes, though calculators are allowed.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all headphones and watches.
- You have 50 (+5) minutes to complete this quiz.

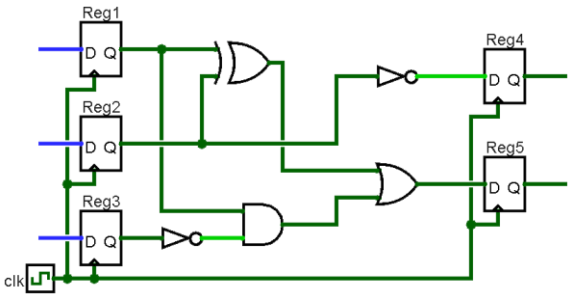
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax.

Static Timing Analysis [10 pts]

setup slack = $DRT_{su} - DAT_{su}$ = min clock path – max data path
hold slack = $DAT_h - DRT_h$ = min data path – max clock path

We will analyze the following circuit with the indicated timing constants:



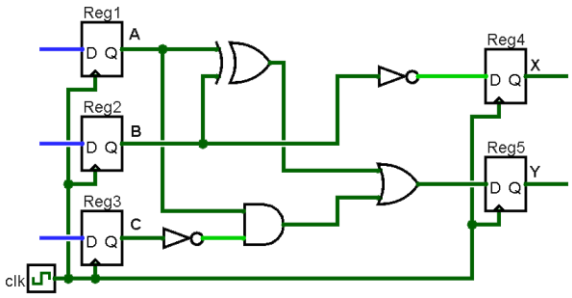
$T = 160$ ns (period), $t_{su} = 15$ ns (all regs)
$t_{wire} = 0$ (all wires), $t_h = 11$ ns (all regs)
$t_{clk1} \in [3, 7]$ ns (Reg1), $t_{CO} \in [12, 16]$ ns (all regs)
$t_{clk2} \in [2, 6]$ ns (Reg2), $t_{NOT} \in [9, 10]$ ns
$t_{clk3} \in [1, 5]$ ns (Reg3), $t_{AND} \in [45, 50]$ ns
$t_{clk4} \in [4, 8]$ ns (Reg4), $t_{OR} \in [45, 50]$ ns
$t_{clk5} \in [3, 7]$ ns (Reg5), $t_{XOR} \in [63, 70]$ ns

Solve for the setup slack and hold slack for this circuit and put your answers in the boxes below. You are allowed to use a calculator on this problem, but no credit will be given without work.

Setup Slack:	ns
Hold Slack:	ns

Pipelining [12 pts]

We will look at a simplified version of the same circuit:



$t_{su} = t_h = t_{wire} = t_{clk} = 0$

$t_{CO} = 16$ ns (all regs)

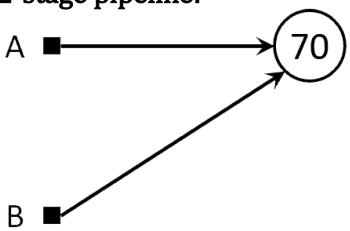
$t_{NOT} = 10$ ns

$t_{AND} = t_{OR} = 50$ ns

$t_{XOR} = 70$ ns

1) **Complete *both copies* of the Data Flow Graph (DFG) for the circuit** by adding nodes labeled with their delays and edges. Note that A, B, C, X, and Y correspond to the labeled nets in the circuit above. One node, corresponding to the upper XOR gate, has been provided for you.
2) **Draw cutsets on your two DFGs to make a 2-stage pipelined and a 3-stage pipelined version of this circuit with *minimal clock period*.** The signals X and Y should remain in sync.
3) Assuming we use the minimum clock periods, **compute the latency** for both pipelined versions of this circuit and write them into the boxes below. No credit will be given without work.

2-stage pipeline:

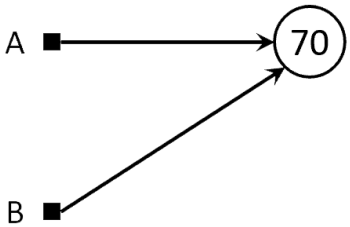


■ X

■ Y

Latency: ns

3-stage pipeline:



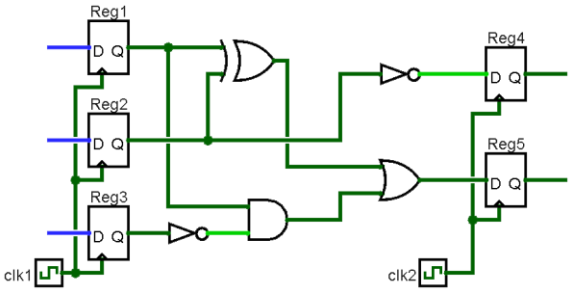
■ X

■ Y

Latency: ns

Clock Domain Crossing [4 pts]

We tweaked the circuit so that Reg4 and Reg5 are now controlled by a separate clock with $T_2 = 3 \times T_1$ (*i.e.*, clk1 has a shorter period):



a) How would/might **data loss** manifest itself at this clock domain crossing? Make sure that your answer is specific to this circuit and not just a general definition of data loss.

b) How would/might **data incoherence** manifest itself at this clock domain crossing? Make sure that your answer is specific to this circuit and not just a general definition of data incoherence.

[End of Quiz]