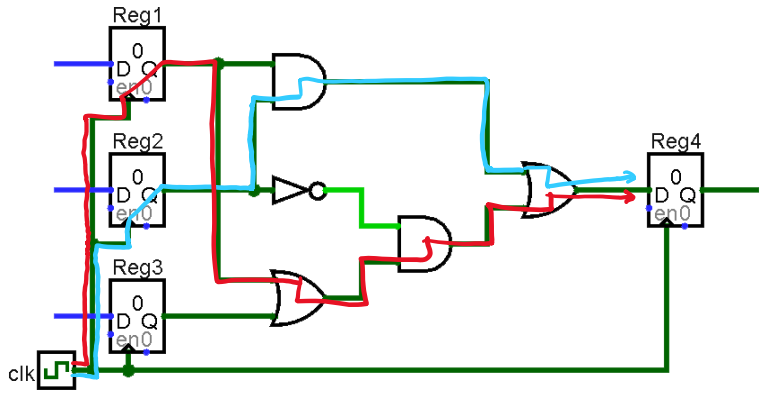
Design of Digital Circuits and Systems, Quiz 5

Timing: STA, Pipelining, CDC

Solution Outlines

Static Timing Analysis:



Longest data path and **shortest data path** are shown on the circuit diagram above (note that the clock network delays are ordered $t_{clk1} > t_{clk2} > t_{clk3}$). Both paths have Reg4 as their destination register for the clock paths.

setup slack = min clock path – max data path

$$= (T + t_{clk4,min} - t_{su,max}) - (t_{clk1,max} + t_{CO,max} + 4 \cdot t_{wire,max} + 2 \cdot t_{OR,max} + t_{AND,max})$$

$$= (200 + 4 - 13) - (7 + 16 + 4 \cdot 0 + 2 \cdot 60 + 50) = \textbf{–2 ns}$$

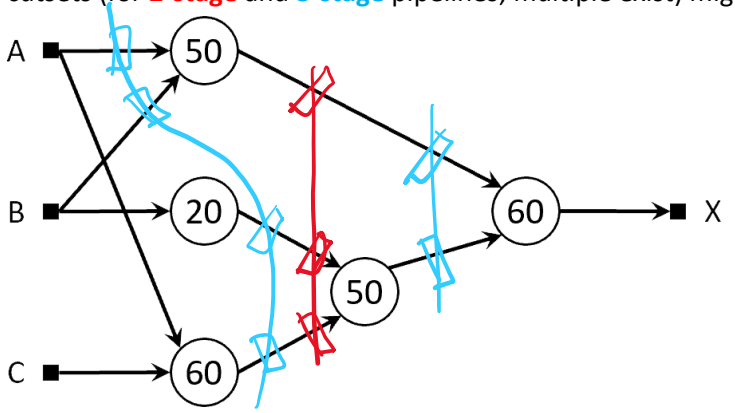
hold slack = min data path – max clock path

$$= (t_{clk2,min} + t_{CO,min} + 3 \cdot t_{wire} + t_{AND,min} + t_{OR,min}) - (t_{clk4,max} + t_{h,max})$$

$$= (2 + 12 + 3 \cdot 0 + 45 + 55) - (8 + 9) = \textbf{97 ns}$$

Pipelining:

The DFG and example cutsets (for **2-stage** and **3-stage** pipelines; multiple exist) might look like:



The key is to break up the critical path along the bottom; the NOT gate must be in the 1st stage while the upper AND gate can be placed in the 1st or 2nd stage as long as it isn't part of the new critical path.

The new 2-stage critical path gives us a T_{min} of $t_{CO} + t_{OR} + t_{AND}$ = $10 + 60 + 50$ = **120 ns**, so the throughput is **1 / (120 ns)**. Since it takes 2 clock cycles for the inputs to reach the output, latency = $2 \cdot T_{min} + t_{CO}$ = **250 ns**.

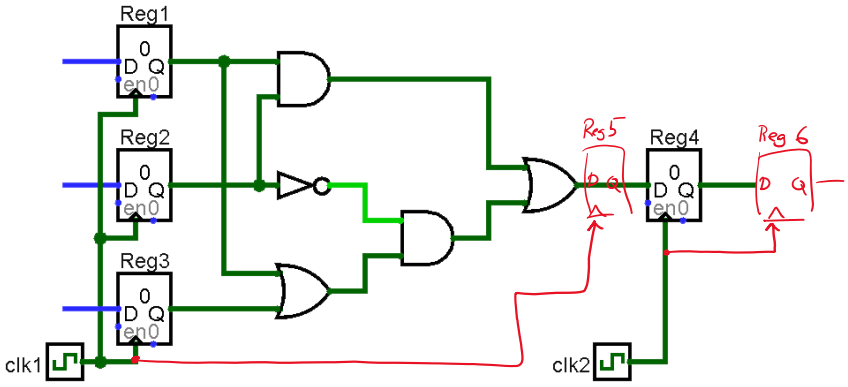
The new 3-stage critical path gives us a T_{min} of $t_{CO} + t_{OR}$ = **70 ns**, so the throughput is **1 / (70 ns)**. Since it takes 3 clock cycles for the inputs to reach the output, latency = $3 \cdot T_{min} + t_{CO}$ = **220 ns**.

The 3-stage pipeline is better in both latency and throughput!

Clock Domain Crossing:

We have a *synchronous* clock domain crossing from a slower sending clock domain to a faster receiving clock domain. The simplest changes to make are:

- Synchronize the sending clock domain by adding a register (Reg5) connected to `clk1` between the last OR gate and Reg4 to reduce the frequency that the input to Reg4 can change.
- Handle metastability in the receiving clock domain by adding a register (Reg6) connected to `clk2` to net X to create a 2-register synchronizer.



- Other answers may receive credit based on their appropriateness to the given CDC.