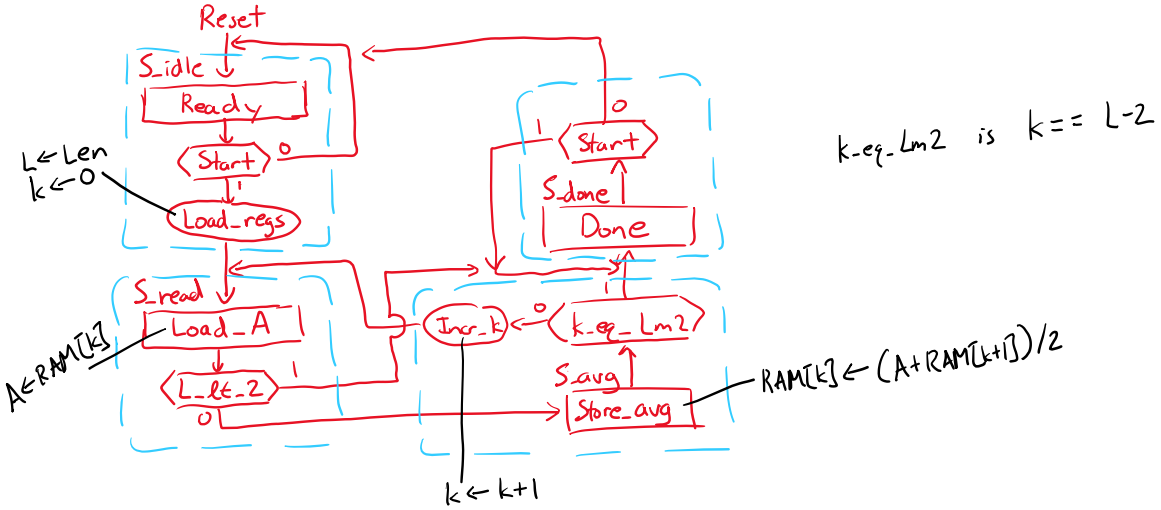
Design of Digital Circuits and Systems, Quiz 4

Algorithms to Hardware

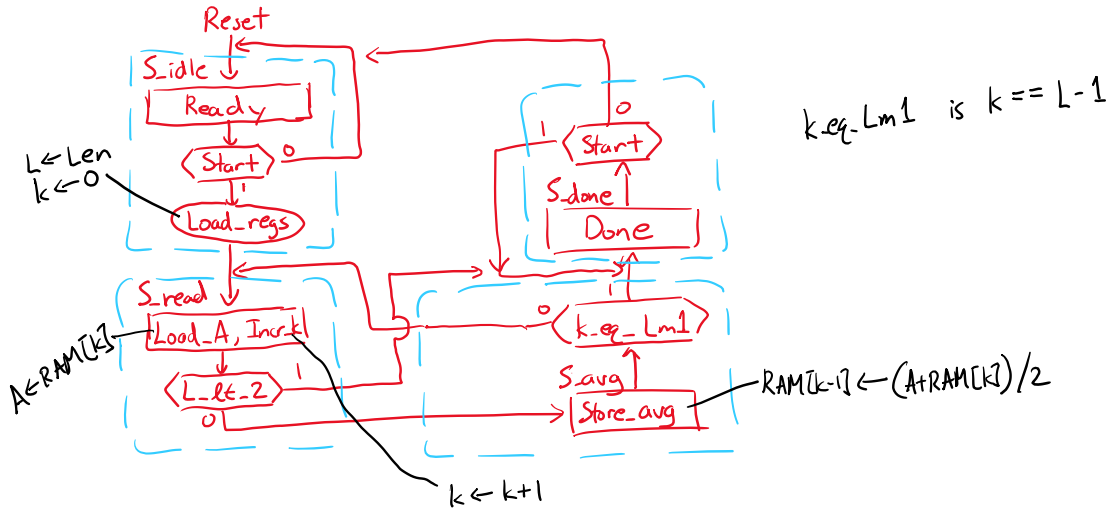
Solution Outlines

Algorithm to ASMD:

Sample Solution 1 (increment after averaging):



Sample Solution 2 (increment before averaging):



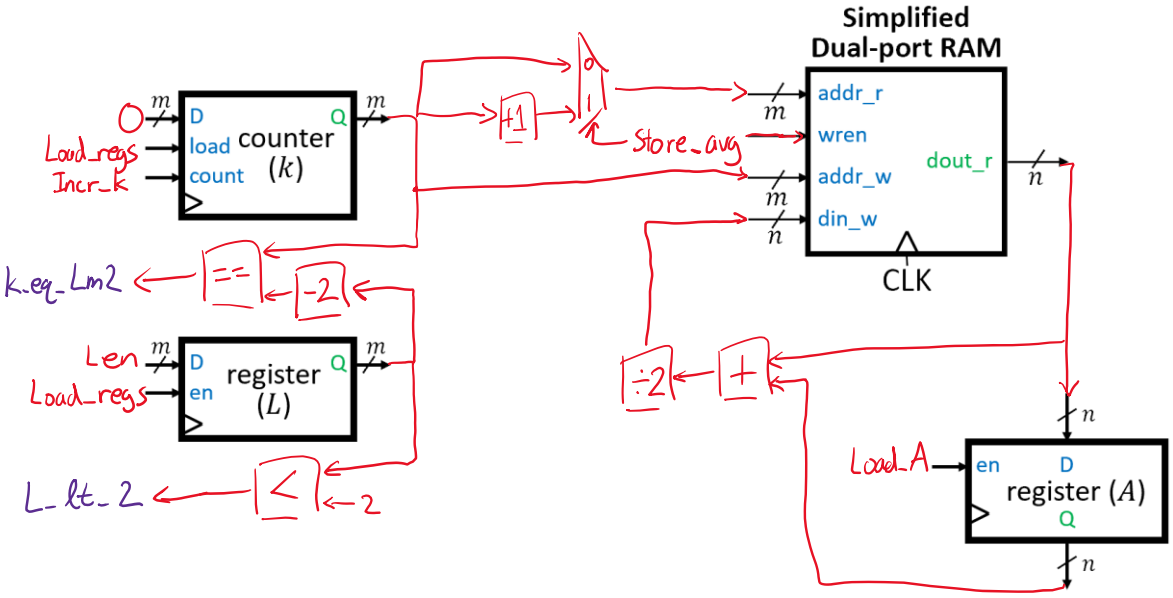
In addition to freedom over the control signal names, acceptable ASMD chart variants include:

- `Load_regs` could have been asserted on the other branch out of the decision box.
- `L<2` check (called `L_lt_2` here) could have been placed after `Start` check in `S_idle`.
- The end condition status signal (called `k_eq_Lm1/Lm2` here) could have been expressed differently (*e.g.*, `lt` instead of `eq` with swapped paths).

Partial Datapath:

- Control and status signal names would depend on ASMD chart from Question 1.
- We did not expect you to show the clock connections, even though everything would need to be connected to the same clock.

Sample Solution 1 (increment after averaging):



Sample Solution 2 (increment before averaging):