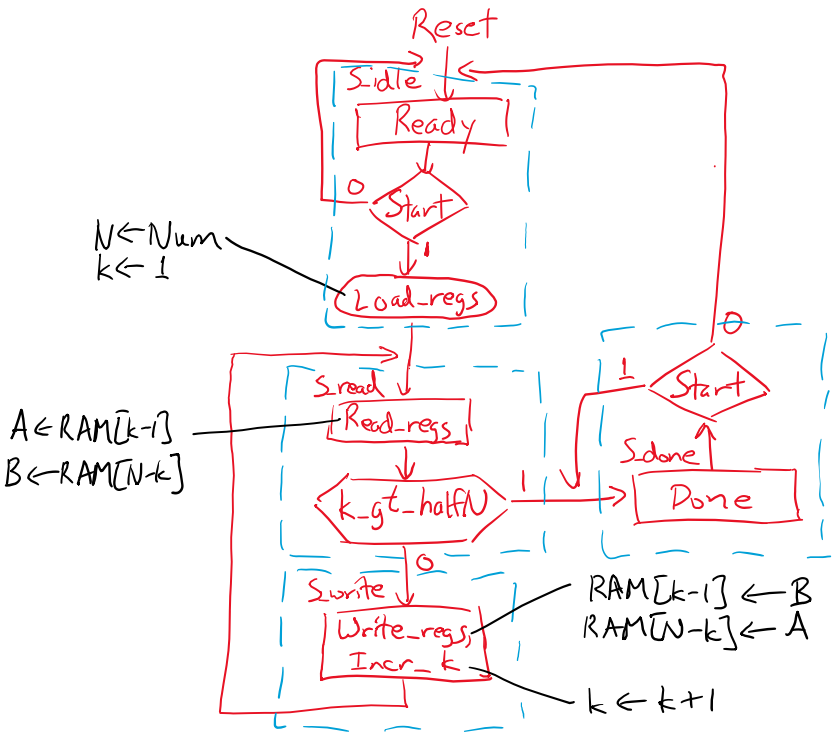
Design of Digital Circuits and Systems, Quiz 4

Algorithms to Hardware

Solution Outlines

Algorithm to ASMD:



In addition to freedom over the control signal names, there are a number of acceptable ASMD chart variants:

- `Load_regs` could have been asserted on the other branch out of the decision box.
- `Incr_k` could have been put in a conditional output box or combined with the `Write_regs` control signal (though that's less readable).
- The `k_gt_halfN` status signal (which checks `k > N/2`) could be checked elsewhere, but would need to be checked in multiple places (*e.g.*, while exiting `S_idle` and in `S_write`).

Partial Datapath:

We did not ask you to draw the status signals, but those would normally be included in a datapath diagram.

- Control signal names would depend on ASMD chart from Question 1.
- Could have also switched the port usage as long as they were crossed (*e.g.*, `dout_a` → `A/B` → `din_b`).
- We did not expect you to show the clock connections, even though everything would need to be connected to the same clock.