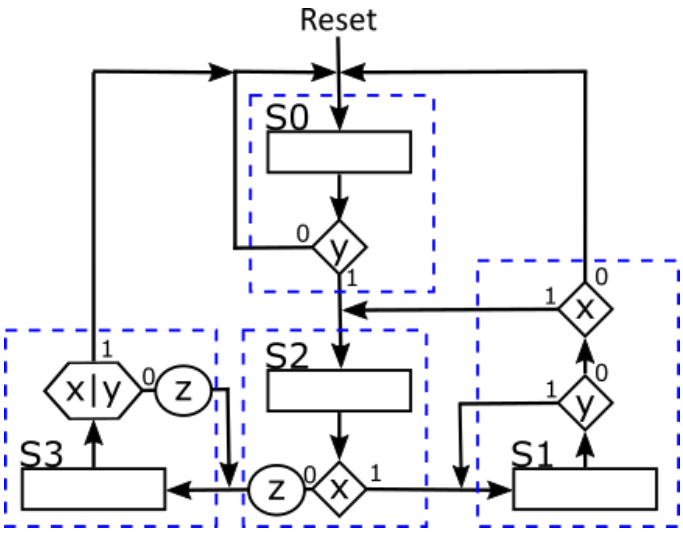
Design of Digital Circuits and Systems, Quiz 3

ASM and ASMD

Solution Outlines

Question 1:



Question 2:

- done is asserted before the computation is complete, but we dictated this for simplicity – would normally use a 5th state (with a start de-assertion loop).
- Alternate names could have been chosen for the control signals.
- Any valid use of C (*e.g.*, increment, decrement, different bounds) that counted out n accepted.
- In `S_sum`, `Iterate` can be a Moore-type output (A and C just finish 1 past expected).