University of Washington – College of Engineering

Spring 2026 Instructor: Justin Hsia 2026-04-23

EE/CSE 371 QUIZ 2

Name: _____

Student ID Number: _____

Please do not turn the page until 11:50.

Instructions

- This quiz contains 4 pages, including this cover page. The 4th page is just for scratch work and won't be graded, but should still be turned in. You may additionally use the backs of the pages for scratch work.
- Please clearly indicate (*e.g.*, box, circle) your final answers if a specific box isn't provided.
- The quiz is closed book and closed notes, though a *scientific* calculator is allowed.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all headphones and watches.
- You have 30 (+5) minutes to complete this quiz.

Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax.
- Powers of 2, for your reference:

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}
1	2	4	8	16	32	64	128	256	512	1024

- IEC prefixes, for your reference:

2^0	2^{10}	2^{20}	2^{30}	2^{40}	2^{50}	2^{60}	2^{70}	2^{80}
—	Kibi	Mebi	Gibi	Tebi	Pebi	Exbi	Zebi	Yobi

Memory Size

Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table representing the following combinational circuit component:

The 4-bit to 8-bit extender circuit from Lecture 2 that can zero- (add `0`'s) and sign-extend (copy most significant bit), as requested.

Depth (in words): _____

Width (in bits): _____

Memory Addressing

We need a memory with a **2 Ki-byte** (not bits) capacity, but only have access to **8 × 64 RAM chips**.

(A) How many of these chips are needed to provide the desired memory capacity?

_____

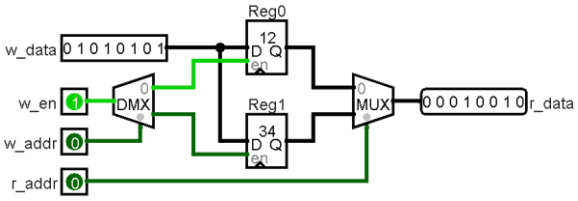
(B) With a 64-bit word size, the overall memory uses 8 address bits, numbered `[7:0]`. Which bits, written using SystemVerilog range notation `[#:#]` (inclusive), are connected to the RAM chips?

`[ : ]`

Memory Implementation

For reference, the implementation of a 1-port, 2 × 8 register file/RAM is given here:

- `D` and `Q` are the register input/output ports
- `en` is the register enable port
- `clk` input (△) connected but not shown
- `MUX` and `DMX` stand for (de)multiplexor

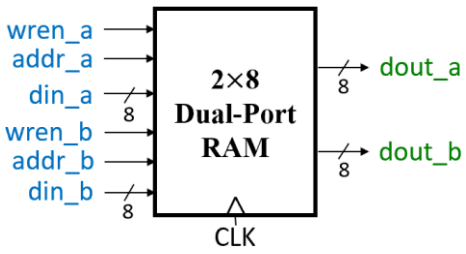


The SystemVerilog code for the writing logic is shown on the right:

```
always_ff @(posedge clk)
  if (w_en)
    RAM[w_addr] <= w_data;
```

We now examine a 2×8 dual-port RAM *as a register file*, which allows for reading and writing from ports a and b simultaneously:

When we have a **write conflict** (*i.e.*, when both ports simultaneously write to the same address), we want to **do nothing (*i.e.*, don't write)**.



(A) Complete the SystemVerilog writing logic below:

```
always_ff @(posedge clk) begin




end
```

(B) Fill out a partial implementation for **just the register enable inputs** (*i.e.*, which input combinations cause each register to update?). Warning: this is NOT a direct translation of the code above.

Space for scratch work. Anything below this line won't be graded.

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