University of Washington – College of Engineering

Spring 2024 Instructor: Justin Hsia 2024-04-18

EE/CSE371 QUIZ 2

Name: _____

Student ID Number: _____

Please do not turn the page until 11:50.

Instructions

- This quiz contains 4 pages, including this cover page. The 4th page is just for scratch work and won't be graded, but should still be turned in. You may additionally use the backs of the pages for scratch work.
- Please clearly indicate (*e.g.*, box, circle) your final answers if a specific box isn't provided.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all headphones and watches.
- You have 30 (+5) minutes to complete this quiz.

Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax.
- Powers of 2, for your reference:

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}
1	2	4	8	16	32	64	128	256	512	1024

Memory Size

Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table representing the following combinational circuit component:

A 4-bit *bidirectional* rotator circuit that can rotate-right or rotate-left by the specified number of bits (*e.g.*, `4'b0001` rotated right by `1` bit outputs `4'b1000`). Assume that the rotation amount must be in the range of 0 to one less than the data bit width.

Depth (in words): _____

Width (in bits): _____

Memory Addressing

We need a memory with a **512-byte** (not bits) capacity but only have access to **4 × 4 RAM chips**.

(A) How many of these chips are needed to provide the desired memory capacity?

_____

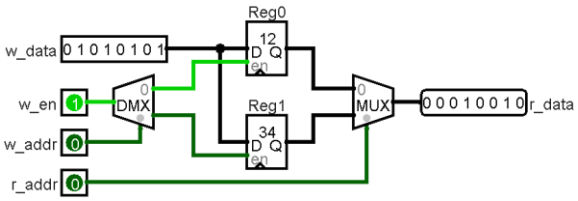
(B) If we want our larger memory to have a word size twice that of our chips, how many address bits/lines will our larger memory require?

_____

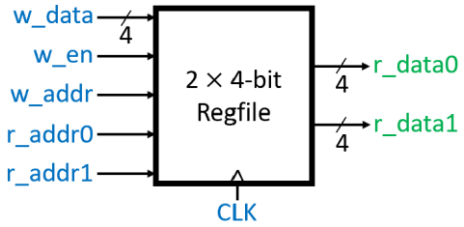
Memory Implementation

For reference, the implementation of a 1-port, 2 × 8 register file/RAM is given here:

- `D` and `Q` are the register input/output ports
- `en` is the register enable port
- `clk` input (△) connected but not shown
- `MUX` and `DMX` stand for (de)multiplexor

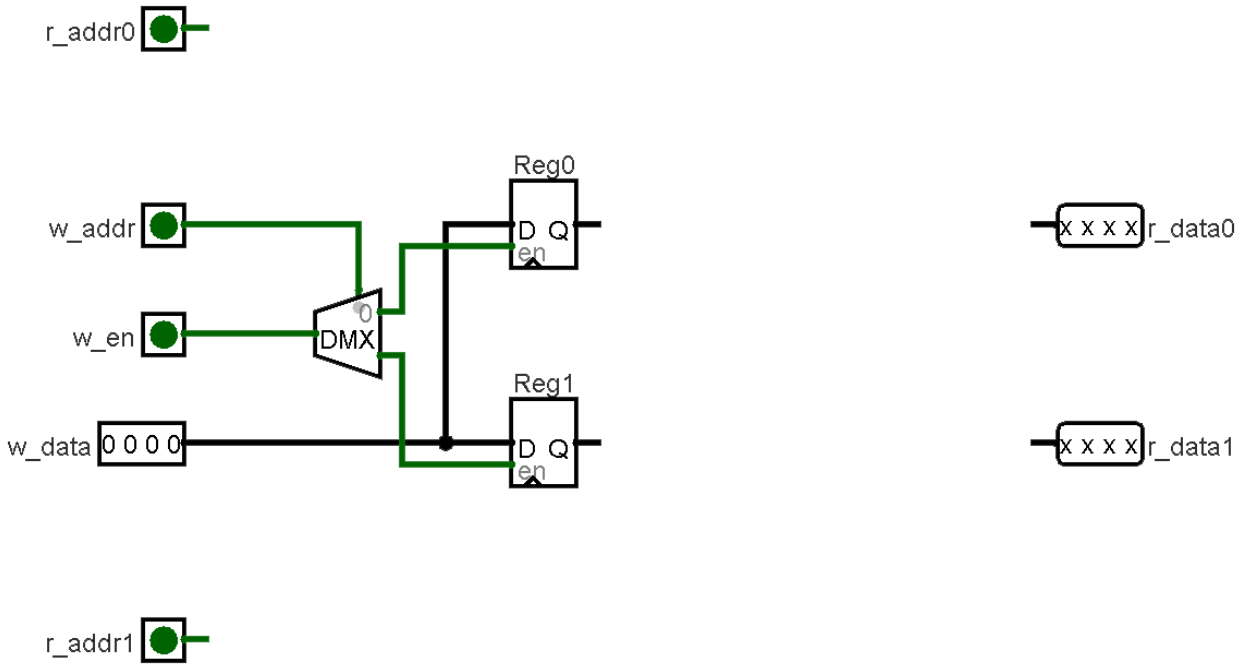


We now examine a register file module with 2 read ports, as introduced in lecture. This configuration allows for reading two values simultaneously.



(A) Complete the implementation of a 2x4 register file with 2 read ports on the next page. Make sure to label your signals and signal widths and what selector combinations correspond to which MUX/DEMUX lines.

- Reading should be *synchronous*.
- In the edge case where we are writing to an address that is being read from, the output should be the *new data* (*i.e.*, r_data ← w_data).



(B) *Briefly* explain your **edge case logic** shown above (*i.e.*, when writing to an address that is being read).

Space for scratch work. Anything below this line won't be graded.

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