Design of Digital Circuits and Systems, Quiz 2

Memory: ROM, RAM, and Register Files

Solution Outlines

Memory Size

4-bit bidirectional rotator circuit: 128 × 4

- Circuit as a 4-bit data input, 2-bit rotate amount (to cover 0-3) and a 1-bit direction input, so 2^7 = 128 total combinations.
- Output width will match data width.

Memory Addressing

Memory capacity of 512 bytes = $2^9 * 2^3 = 2^{12}$ bits.

a) Each 4 × 4 RAM chip holds $2^2 * 2^2 = 2^4$ bits, so we need $2^{12}/2^4$ = 256 chips.

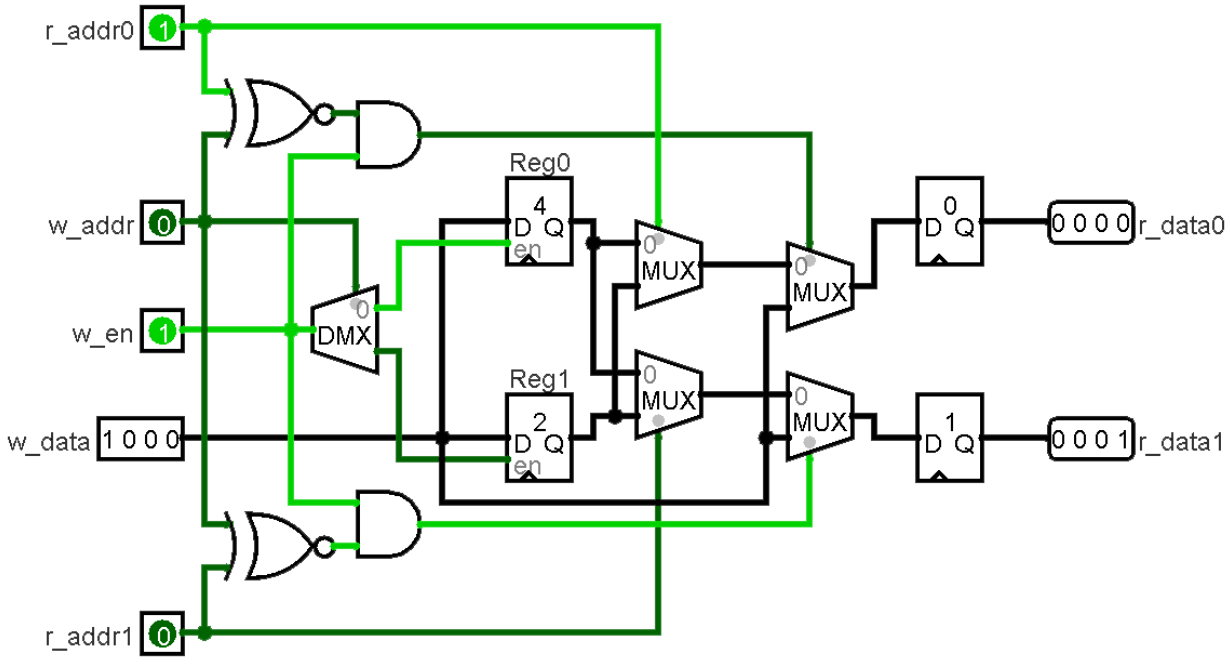
b) Using 8-bit words (1 byte each), our 512-byte memory would be organized as 512 × 8, which requires $\lceil \log_2 512 \rceil$ = 9 address bits.

Memory Implementation

The edge case logic can be expressed in SystemVerilog as:

```
assign r_data0 = ((r_addr0 == w_addr) & w_en) ? w_data : (r_addr0 ? reg[1] : reg[0]);
```

In the edge case (addresses match AND we are writing), we pass `w_data`, otherwise we pass the register data. This is equivalent to two cascading 2:1 MUXes, as seen below.



Notes:

- The clock connections are not shown but would need to be there in the actual circuit.
- The rightmost registers synchronize the outputs, which means that the requested data shows up 1 clock cycle later.