University of Washington – College of Engineering

Spring 2023 Instructor: Justin Hsia 2023-04-20

EE/CSE371 QUIZ 2

Name: _____

Student ID Number: _____

Please do not turn the page until 11:50.

Instructions

- This quiz contains 4 pages, including this cover page. The 4th page is just for scratch work and won't be graded, but should still be turned in. You may additionally use the backs of the pages for scratch work.
- Please clearly indicate (*e.g.*, box, circle) your final answers if a specific box isn't provided.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all headphones and watches.
- You have 30 (+5) minutes to complete this quiz.

Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax.
- Powers of 2, for your reference:

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}
1	2	4	8	16	32	64	128	256	512	1024

Memory Size

Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table representing the following combinational circuit component:

A circuit component that counts the number of "0" bits in a 4-bit input (*e.g.*, `4'b0001` outputs `3`, `4'b1010` outputs `2`). Assume that the output width is the minimum required.

Depth (in words): _____

Width (in bits): _____

Memory Addressing

We need a memory with a **256 byte** (not bits) capacity but only have access to **16 × 8 RAM chips**.

(A) How many of these chips are needed to provide the desired memory capacity?

_____

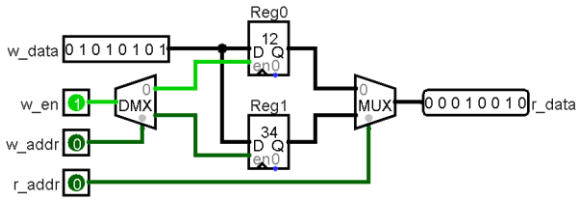
(B) How many address bits/lines will our memory require to decode our chip select (*i.e.*, how many address bits are needed for us to know which RAM chip we need to access)?

_____

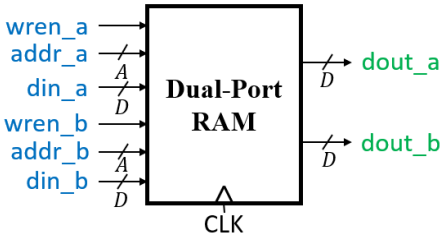
Memory Implementation

For reference, the implementation of a 1-port, 2 × 8 register file/RAM is given here:

- `D` and `Q` are the register input/output ports
- `en` is the register enable port
- `clk` input assumed, but not shown
- `MUX` and `DMX` stand for (de)multiplexor

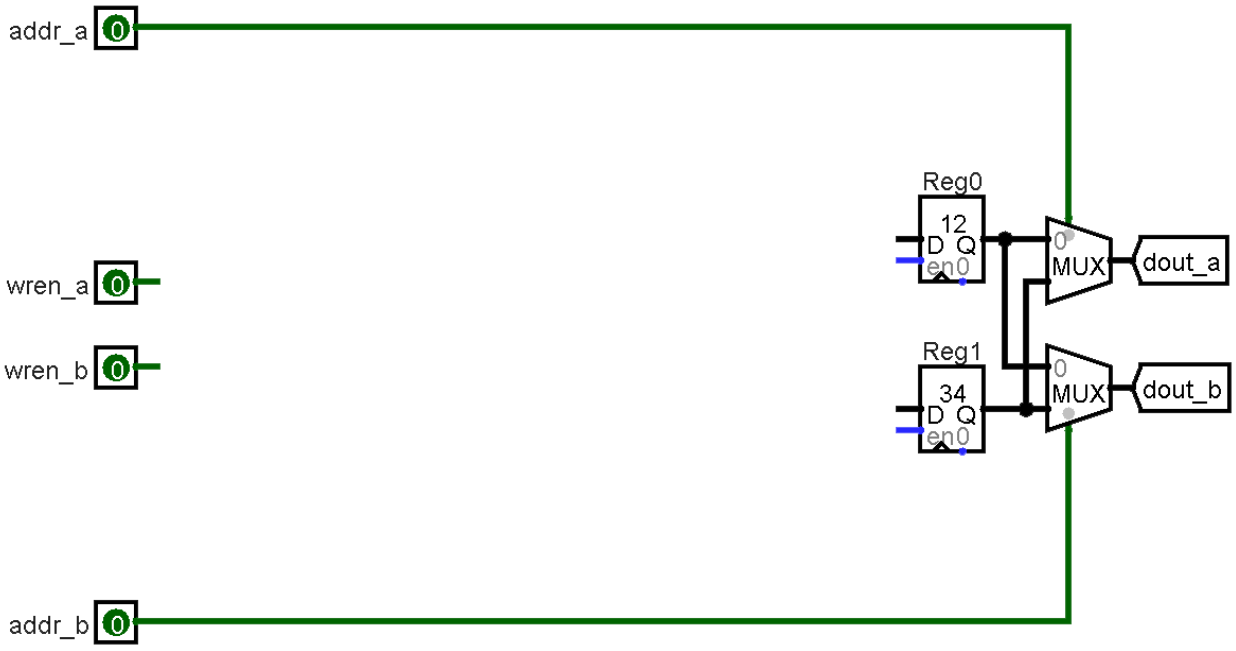


We now examine a dual-port RAM module, as introduced in lecture. This configuration allows for either reading or writing from ports `a` and `b` simultaneously.



(A) Complete the implementation of a 2x8 dual-port RAM *as a register file* on the next page. Make sure to label your signals and signal widths and what selector combinations correspond to which MUX/DEMUX lines.

- For the ports not shown (`din_a`, `din_b`), you can write their names next to any wire you want to connect them to (as shown with `dout_a` and `dout_b`).



(B) *Briefly* explain how you chose to handle **write conflicts** (*i.e.,* when both ports simultaneously write to the same address).

Space for scratch work. Anything below this line won't be graded.

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