Design of Digital Circuits and Systems, Quiz 2

Memory: ROM, RAM, and Register Files

Solution Outlines

Memory Size

A circuit that counts the number of 0 bits in a 4-bit input: 16 × 3

- A 4-bit input has 2^4 = 16 total combinations.
- In 4 bits, you can have anywhere from 0 (`0b0`) to 4 (`0b100`) 0's, so you need 3 output bits.

Memory Addressing

Memory capacity of 256 bytes = $2^8 * 2^3 = 2^{11}$ bits.

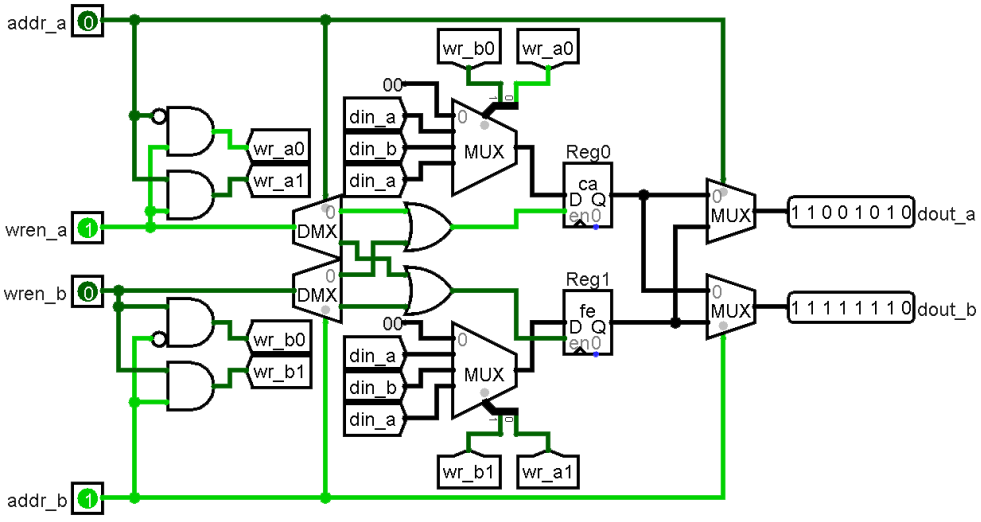
a) Each 16 × 8 RAM chip holds $2^4 * 2^3 = 2^7$ bits, so we need $2^{11}/2^7$ = 16 chips.

b) Since we have 16 chips, we need $\lceil \log_2 16 \rceil$ = 4 address bits connected to a 4:16 decoder to select between them.

Memory Implementation

Both solutions below rely on giving *priority* to one of the ports (Port A) when there is a conflict. There are many logically-equivalent solutions that will work.

Sample Solution 1: MUX-based priority logic. Probably the more logically straight-forward solution, but lots of wiring needed.

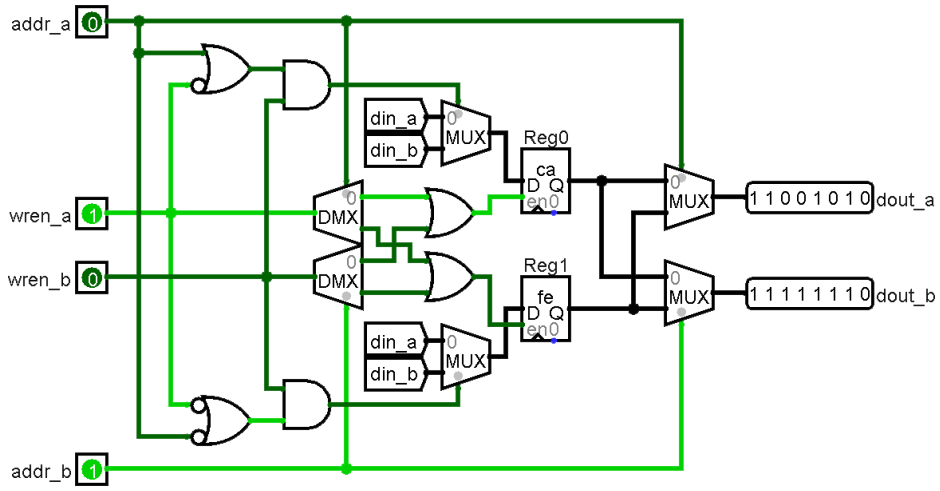


Notes:

- The clock connections are not shown for the registers, but would need to be there.
- A register should be enabled if either port wants to write to it.

- The intermediate signals `wr_a0`, `wr_a1`, `wr_b0`, `wr_b1` represent whether Port A or B are trying to write to Reg 0 or 1.
- The ordering of the MUX inputs would depend on your choice of the ordering of the MUX selector bits. The `0b00` input is a don't care, though we are choosing to use `0x00` here.

Sample Solution 2: Selector bit-based priority logic. The smaller circuit generated by using 2:1 MUXes on the register inputs and then using K-maps on `wren_a`, `addr_a`, `wren_b`, and `addr_b` to solve for the MUX selector bit logic.



Notes:

- As there were 9 don't cares in each K-map and the bit encoding of `din_a` and `din_b` could have been reversed, there are many other correct versions of the selector bit logic.