DesignWorks™ for Windows
Hands-On Demo Guide

Schematic and Simulation Version 3.1.1 August 1994

406 - 960 Quayside Drive
New Westminster, B.C., Canada, V3M 6G2
(604) 522-6200

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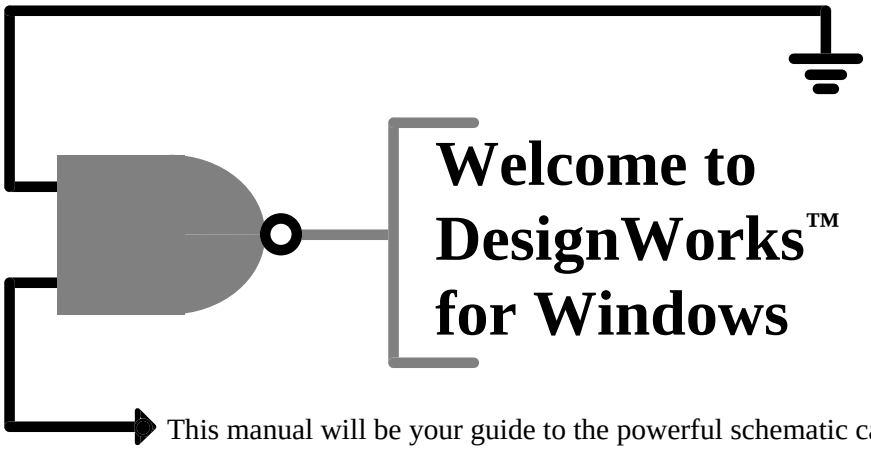


Welcome to DesignWorks™ for Windows

This manual will be your guide to the powerful schematic capture features of the DesignWorks package. After just a few minutes, you will be creating complete schematic diagrams, generating netlist output, creating your own device symbol libraries and building a hierarchical design.

To allow you to get a quick overview and then delve into specific topics of interest, this manual is divided into the following sections:

- The 5-Minute Schematic
- The 5-Minute Simulation
- Advanced Schematic Editing
- Creating Device Symbols and Hierarchical Design
- Using DesignWorks with SPICE-based Simulators
- Advanced Simulation
- Editing and Execution Test Vectors
- Other Schematic Features
- Other Simulation Features

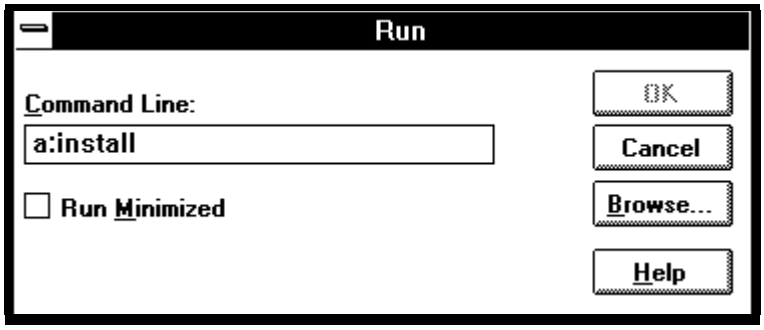
Note: All sections build on the information presented in the 5-Minute schematic tutorial. It is recommended that this section be reviewed first.

Quick Installation

Note: If you are using this manual in conjunction with the complete DesignWorks package, please see the Release and Installation Notes provided with the package for installation instructions.

To install the demonstration version:

- Make sure you have about 5 megabytes of disk space free on your hard disk.
- Insert the diskette into drive "a" of your machine.
- Select "Run" from the Program Manager's File menu and enter "a:install". If the disk was inserted in any other drive then substitute the correct drive letter.



- Follow the instructions displayed by the installer.

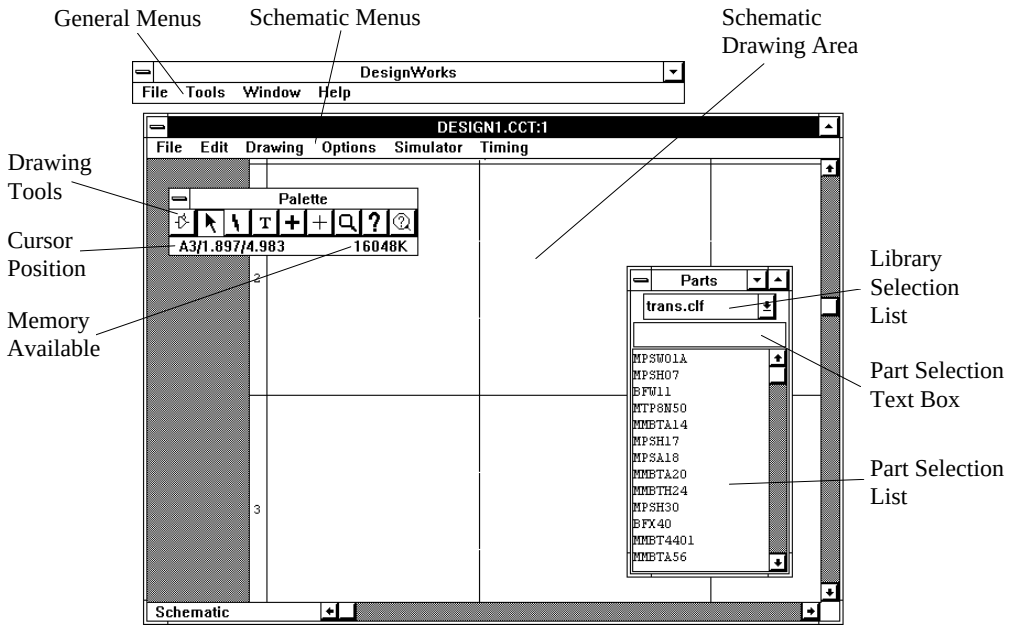
The installer will create a program group called "DesignWorks Demo" (or similar) on your disk. To start the program, just double click on the DesignWorks Demo icon.

Note Regarding Libraries:

If you are using a demonstration version of DesignWorks, only a small sampling of parts libraries are provided due to disk space limitations. All the parts required for these tutorials are included, but the listings you see on the screen in the Parts palette may vary from those shown in this guide.

The Appendix at the back of this manual lists the complete set of libraries provided with DesignWorks.

The DesignWorks Screen



Drawing Tools

Symbol	Tool	Description
	Pointer	Used to select or drag objects and extend signals.
T	Text	Used to name a signal or device to name, or to place text notations on the schematic.
	Zap	Used to remove single objects. Press the button to remove whatever the tip of the cursor is pointing at.
+	Draw Bus	Used to create a new bus line or extend an existing bus.
+	Draw Sig	Used while creating a new signal line or extending an existing signal.
	Magnify	Used to zoom in and out. Clicking on a point or dragging down and right zooms in, dragging up and left zooms out.
?	Attribute Probe	When the "dot" portion of the cursor is clicked on a device, pin or signal, the contents of the attribute fields for that object are displayed.
	Logic Probe	When the probe end is clicked and held on a signal or pin the current simulation logic level of the signal or pin is displayed.

Manual Format

In all of the following sections, action instructions are shown in **bold face like this**, whereas explanatory text is shown in normal typeface.

Mouse Instructions

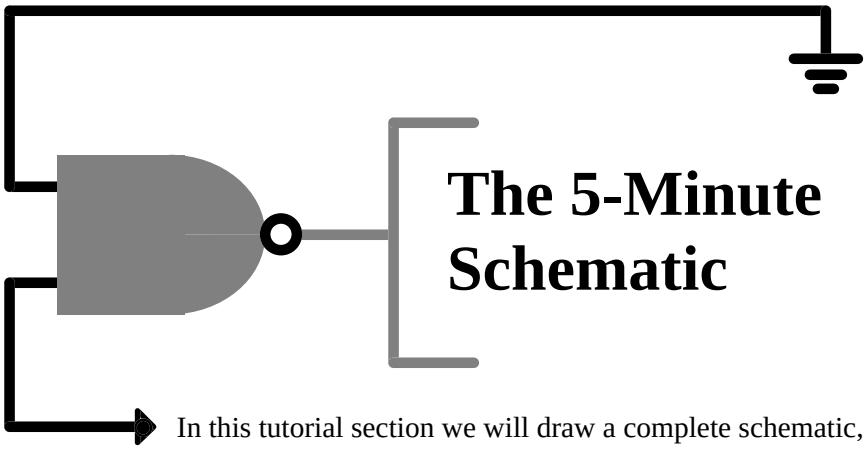
In this manual, the following terms will be used for mouse operations:

Click	Press and release the left mouse button with the mouse held in the same position.
Double-click	Press and release the left mouse button twice in quick succession.
Click and Hold	Press the left button and hold it pressed until a subsequent instruction tells you to release it.
Click and Drag	Press the left mouse button and hold it pressed while moving it to a new location. Release the button when the cursor is positioned at the desired final location.
Right-click	Press and release the right mouse button to display a pop-up menu. A menu item may then be selected with the left mouse button.

Keyboard Usage

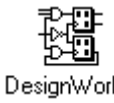
The following special keys on the keyboard are commonly used in DesignWorks editing operations:

Arrow (cursor) Keys	The arrow keys are used to set the orientation of device symbols or clipboard scraps while in placement mode.
Spacebar	As long as no text entry is active, the spacebar resets the cursor to the normal pointer mode.



The 5-Minute Schematic

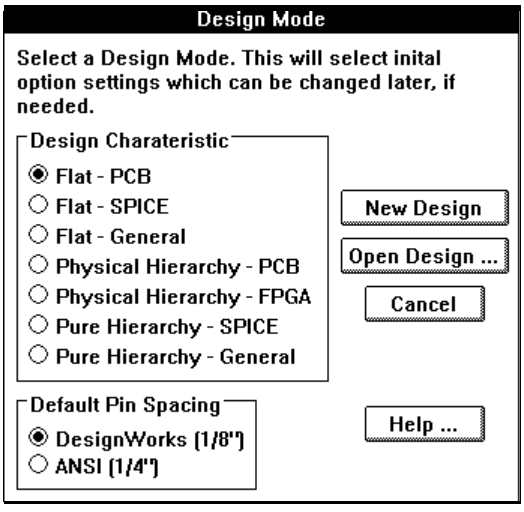
In this tutorial section we will draw a complete schematic, ready for PCB layout.



Starting the Program

• If it is not already running, double-click on the DesignWorks™ icon to start the program.

After loading the program and opening libraries, you will see the Design Mode dialog.



Creating a New Design

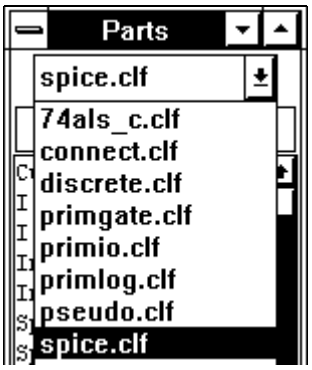
The Design Mode dialog allows you to select a design mode based on your application. Each selection enables the group of options most commonly used for the application type. All options can be changed later, if desired.

• Select the "Flat - PCB" mode.

• Click on the New Design button.

We have selected a mode which enables PCB auto-packaging functions and assumes a flat (i.e. non-hierarchical) design.

You will now see an empty schematic drawing window similar to the one described earlier in this manual.

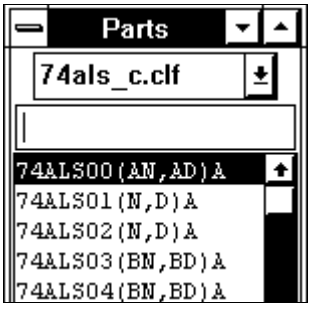


Choosing a Library

• Move the cursor to the library selection drop-down list and choose the "74als_c.clf" library.

The contents of this library will now be displayed in the part selection list.

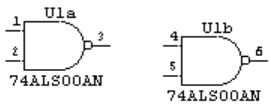
Note: If you are using the demonstration version of DesignWorks, the exact parts listing may vary from what is shown here.

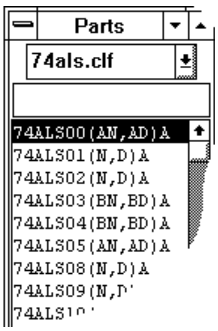


Selecting a Part

• Move the cursor to the part selection list and double-click on the item "74ALS00(AN,DN)A". Move the cursor into the schematic drawing area.

You will see a flickering image of the selected part following the cursor movement. This part does not become a permanent part of the schematic until you click the mouse button.





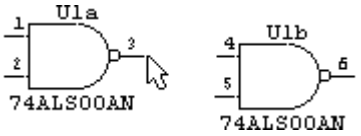
Placing a Device

• Move the cursor to an area just left of the parts palette and click on the schematic area to place a device.

• Move and click again to place a second device as shown. Order of placement is not important.

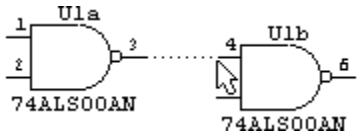
You can continue to place devices of the same type just by clicking on the desired locations. Notice that each device is automatically labeled with its part type and package assignment. This automatic assignment can be disabled if desired.

• Return to the normal pointer by pressing the spacebar.



Wiring Pins

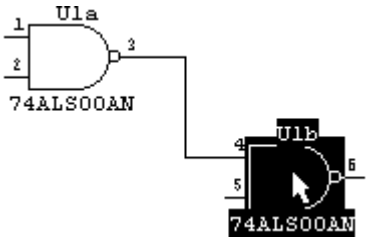
• Move the pointer cursor exactly to the end of the output pin on the left-hand device, as shown, then click and hold the mouse button.



Wiring Pins (cont'd)

• With the mouse button still held down, move the cursor to the right, away from the output pin, so that it is positioned exactly over the end of the upper input pin of the right-hand device. Release the mouse button.

You will see the signal line flash briefly indicating that a connection has been made.



Moving Devices

• Click and drag on the right-hand device and move it to a new position, as shown.

Notice that the connected signal line stays attached and stretches to follow the device movements.

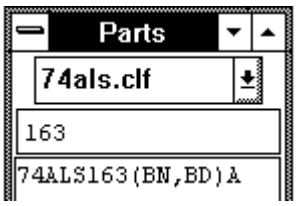
Using Undo/Redo

• Select the Undo command from the Edit menu.

• Select the Undo command again, and repeat until all items you have placed have disappeared.

• Now select the Redo command and repeat it until all edits are redone.

Most schematic editing operations can be undone and redone up to 10 levels. Major structural changes (like adding a page or hierarchy level) or any operation involving a dialog cannot be undone.



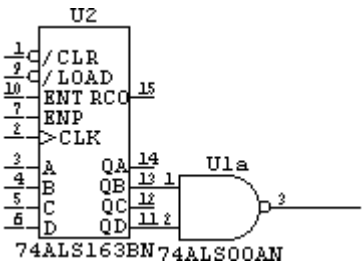
Part Selection by Name

• Click on the part selector text box in the Parts Palette.

You will notice a text cursor starts to flash in this box.

• Enter the value 163.

• Double-click on the part "74ALS163(BN,BD)A" in the list.

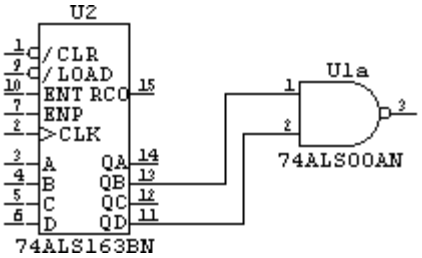


Automatic Pin Connection

• Move the cursor so that you can place the 74ALS163 device exactly as shown so that the QB and QD pins just touch the two inputs on the NAND gate.

• Click the mouse button to place the device at this point. (Depending on the size of your screen, you may need to use the scroll bar at the bottom of the schematic window to make room on the left.) You will notice the two pins flash to indicate a connection.

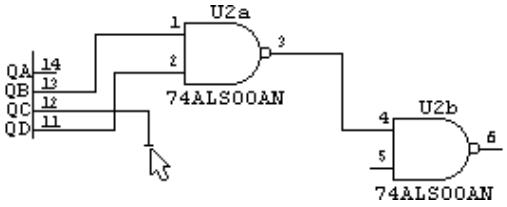
• Press the spacebar to return to the normal pointer.



Automatic Pin Connection (cont'd)

• Click and drag the 74ALS163 device to the left and notice that right-angle lines maintain the connections between the two devices.

This auto-connection feature can be a convenient way of making connections between large devices, such as 8-bit registers. Just place them so the two sets of pins touch, then drag them apart and all the connections are made automatically.



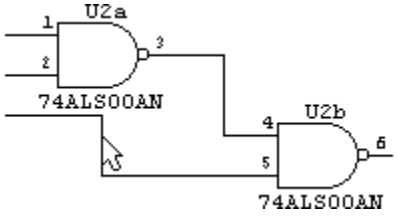
Wire Editing

• Using the pointer ( ) tool, click and hold on the end of output pin QC on the 74ALS163.

• Move to the location shown and release the mouse button. (You may have to modify this procedure slightly depending on the exact positions of your symbols.)

Notice that a small perpendicular mark is placed at the end of the signal line. All unconnected line ends are marked this way automatically to simplify checking for missed connections.

• Click and hold on the end of the line just completed and connect it to the lower pin on the NAND gate.

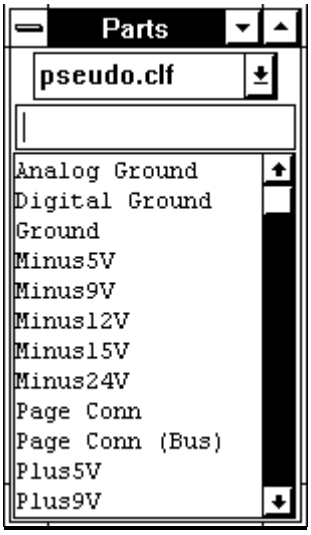


Wire Editing (cont'd)

Note: If you're using a small screen, you can hide the Parts palette at any time by double-clicking in the top left corner of the window. To re-display it, select LibIO from the Tools menu in the DesignWorks window.

• Using the pointer ( ) tool, click and hold at a point midway along the vertical line (or any line) just created.

Notice that you can drag this line segment sideways. With the pointer ( ) tool, clicking at the end of a pin or line segment or at an intersection allows you to extend the signal. Clicking in the middle of a segment allows you to move that segment. The signal drawing tool (+) can be used to draw from any point.



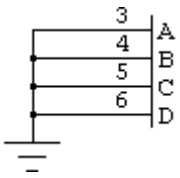
Power and Ground Connections

• If necessary, use the scroll bar at the bottom of the schematic window to expose some drawing area to the left of the 74ALS163 device. (If the device is too close to the left edge of the sheet, select the Custom Sheet Info command from the Drawing menu, and enable the "Auto Expand" option.)

• Go to the library drop-down list and select the "pseudo.clf" library.

The term "pseudo device" is used in DesignWorks to refer to symbols that are edited like devices on the schematic, but are actually symbols used to modify signal connections. Examples of pseudo-devices are power and ground symbols, page connectors and bus breakouts. These items will be discussed in more detail later.

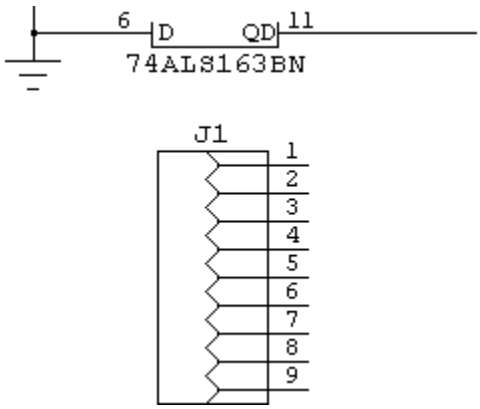
Power and Ground Connections (cont'd)



• Select the Ground item in the parts palette, then place one as shown.

• Click on the signal tool (+) in the tool palette and wire it to the 74ALS163 device as shown.

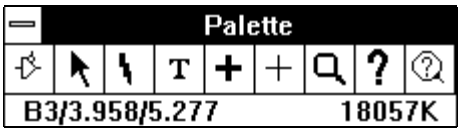
The Ground symbol automatically names the attached net "Ground" and causes it to be logically connected to all other ground nets in the circuit.



Connector Devices

• Select the "connect.clf" library and place a DB9F connector symbol below the 74ALS163, as shown. (Depending on the size of your screen, you may need to scroll the schematic window downwards.)

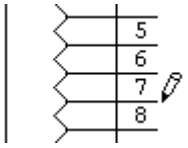
Connectors can be treated as a single unit, as in this case, or broken up into multiple symbols each with 1 or more connector pins on them. In the netlist, these will be treated as a single device.



Connecting Signals by Name

• Click on the text (T) tool in the tool palette.

This tool is used to name devices and signals, edit device pin numbers, edit attribute text or create miscellaneous text notations, depending on where it is clicked. The cursor will initially take on a pencil shape ( ), allowing you to point accurately at the item to be named.

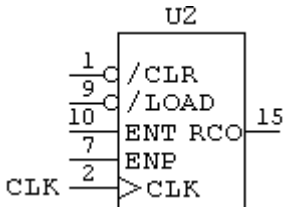


Connecting Signals by Name (cont'd)

• Click on the end of connector pin 7 using the pencil tool.

When you release the button a default name is displayed. Unless auto-naming is disabled, every signal is assigned a unique name as it is created. This name is normally only displayed on the schematic when explicitly requested.

• Enter the name "CLK" and press the Enter key to terminate text entry.



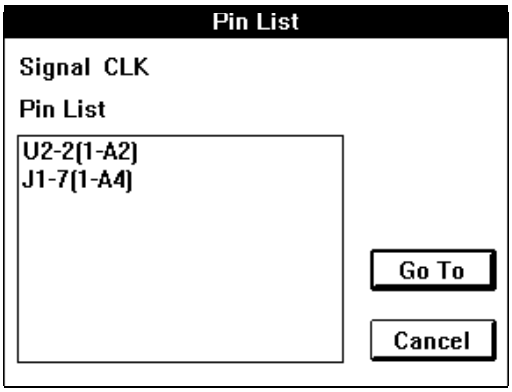
Connecting Signals by Name (cont'd)

• Move to the CLK input on the 74ALS163 device and repeat the same procedure, naming this pin "CLK" as well.

Notice that when you press the Enter key this time, the signal flashes to indicate a connection has been made with the other CLK label.

Confirming Connections

• Press the space bar to return to Point mode.



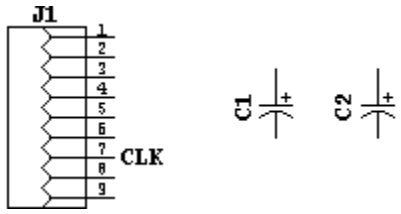
• Click on the name CLK that was just typed so that the name itself and the device pin is highlighted.

• Select the Get Info command from the Options menu. Click on the Pin List button.

(There is a shortcut for this procedure that will be mentioned later.) The Pin List dialog shows you all device pins that are linked by this signal, along with their page number and grid reference.

• Double-click on any item in this list to display it on the screen.

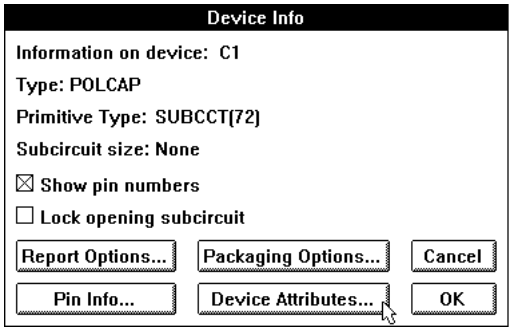
The Pin List dialog will locate items on any page in the circuit, whether connected by signal line, by name, by off-page connector or by bus.



Discrete Components

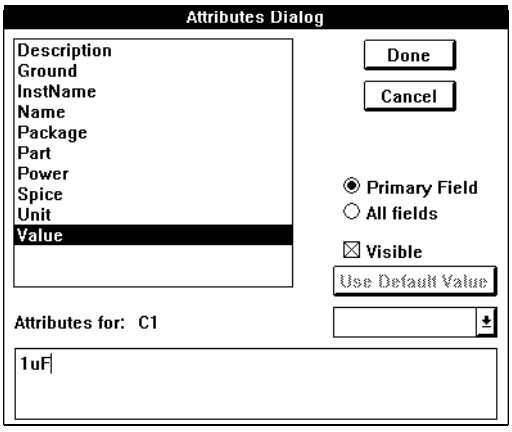
- **Using the library selection pop-up menu, select the "discrete.clf" library. Double-click on the item POLCAP and move the cursor into the schematic area.**
- **Press the arrow keys (or, if you don't have arrow keys, click on the ( ) item in the tool palette and select a new orientation) to orient the symbol vertically.**
- **Place two capacitors as shown.**

Devices can be rotated to one of 8 orientations (the 4 compass points plus mirrored versions of each). Device text notations can optionally be rotated to match the device.



Setting Component Value

- **Click on one of the capacitors just placed, so that it is highlighted.**
- **Choose the Get Info command from the Options menu, then click on the Device Attributes button.**

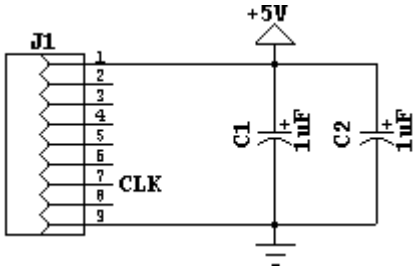


Setting Component Value (cont'd)

This dialog allows you to view and edit text "attributes" of a device. The list at the left shows the available field names. Clicking on one of these will display the associated value in the text box.

- **Click on the item Value in the field list at left. Enter the value "1uF".**
- **Make sure that the Visible box is checked, then click on the Done button then the OK button.**
- **Repeat this procedure to assign the same value to the other capacitor.**

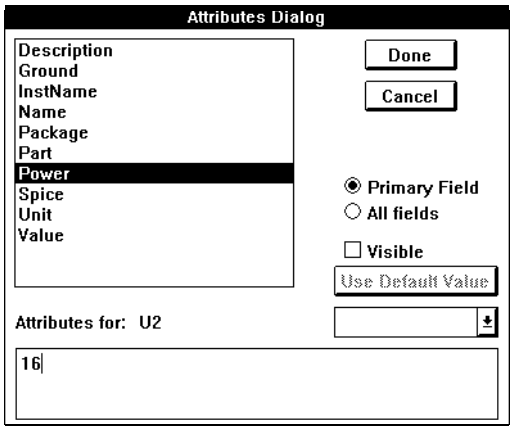
The component value just entered will now appear adjacent to the device. It can be moved around independently, if desired. We will see in a later tutorial how to edit, rotate, hide and set text style for this text.



More on Power and Ground

- **Go back to the "pseudo.clf" library. Place a Ground and Plus5V symbols.**
- **Wire them to the capacitors and connector, as shown. (Note: You may have to use the arrow keys again to return to normal orientation.)**

The Ground and Plus5V symbols are a special class of pseudo-device known in DesignWorks as a "signal connector". They cause all like-named nets to be connected together, even across multiple pages. You can customize your own signal connectors for other types of common connections.



More on Power and Ground (cont'd)

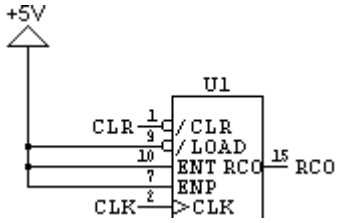
• Click on the 74ALS163 device so that it is highlighted.

• Select the Get Info command from the Options menu, then click on the Device Attributes button.

• Select the field Power in the attribute field list and note the field value.

• Select the field "Ground".

You will notice that the fields named "Power" and "Ground" contain the numbers of the power supply pins for this device. You can add other pins to this list, if needed, separated by commas. This allows you to create power and ground connections without showing them explicitly on the schematic. The standard power and ground connections are included in all integrated circuit parts in the DesignWorks libraries.

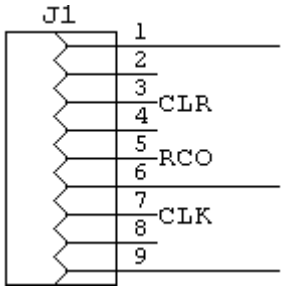


More on Power and Ground (cont'd)

To complete the counter wiring:

• Add a Plus5V symbol and wire it as shown.

• Apply names to the CLR and RCO counter pins, as shown.

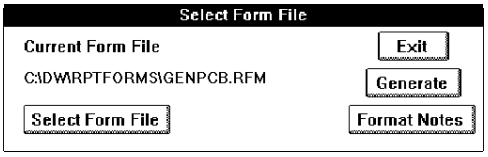


More on Power and Ground (cont'd)

To complete the connector wiring:

• Using the text (T)tool, apply names CLR and RCO to the connector pins shown.

• Using the (+) tool, draw a wire from the unconnected NAND gate output to connector pin 6.



CLK J1-7 U2-2

CLR J1-3 U2-1

Ground C1-2 C2-2 J1-9 U1-7 U2-3 U2-4 U2-5 U2-6 U2-8

Plus5V C1-1 C2-1 J1-1 U1-14 U2-7 U2-9 U2-10 U2-16

RCO J1-5 U2-15

SIG1 U1-1 U2-13

SIG2 U1-2 U2-11

SIG3 U1-3 U1-4

SIG6 J1-6 U1-6

SIG20 U1-5 U2-12

Generating a Netlist

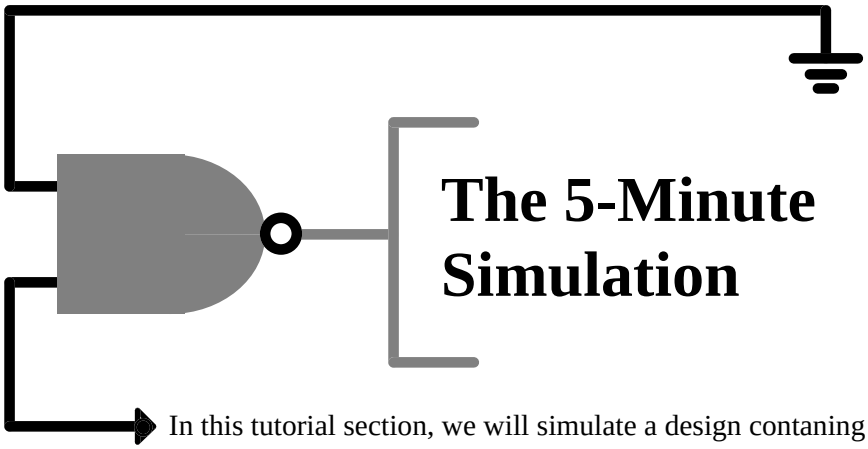
We have now completed our simple schematic and the last step is to generate a netlist for PCB layout purposes.

- **Select Report from the Tools menu in the DesignWorks window.**
- **Click on the Select Form File button.**
- **Using the standard open file dialog, locate the file "genpcb_f.rfm" (or any other PCB form available) in the Rptforms directory.**
- **Click on the Generate button.**
- **Using the standard file save dialog, select a suitable location for the output file.**

You have now saved a text report file that contains a connection list (netlist) for your circuit. Appendix B at the back of this manual describes more features of the report generation tool.

This completes the tutorial section “The 5-Minute Schematic”.

- If you are using a demonstration version of DesignWorks, you will not be able to save the completed circuit, but a similar sample file is provided on the disk.
- If you are using the full DesignWorks package, then you may wish to use the Save As command from the File menu to save the completed example at this point.



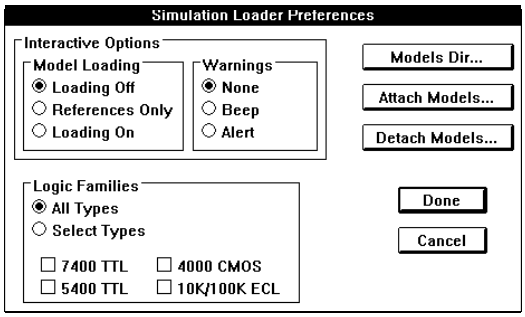
The 5-Minute Simulation

In this tutorial section, we will simulate a design containing standard 74ALS parts and display the results in a timing window.

Starting the Program

- **If it is not already running, double-click on the DesignWorks icon to start the program.**
- **Use the Open Design command to open the demonstration file "5mindemo.cct" provided in the Demo directory OR create it using the instructions given earlier in this manual.**

Note: If the Simulator menu does not appear in the Schematic window when the program is started, then the Simulator is not correctly installed.



Attaching Simulation Models

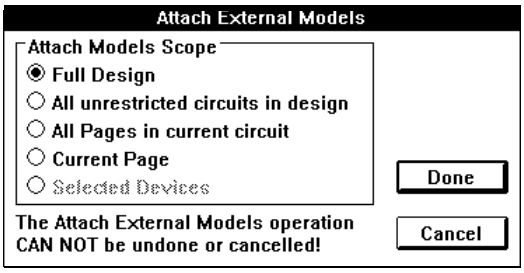
When a design is created without the Simulator option active, the device symbols have no simulation function. In this step, we will locate and attach the simulation models corresponding to each of the 74XX devices in this design.

• Select SimLoad from the Tools menu in the DesignWorks window then click on the Attach Models button.

"Attach Models" allows you to locate models after the design is created.

Attaching Simulation Models (cont'd)

In this case, a "simulation model" is simply a small design file that contains the internal circuit for a given device.



• Click on the Done button in the Attach External Models dialog.

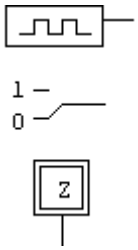
The design will now be scanned and models located for the two 74XX devices in this design. A summary dialog will be displayed when the operation is completed.

• Click on the OK button in the update summary dialog, then click on the Done button in the SimLoad dialog.

Note:

• The demonstration version of the Simulator limits the elapsed time for a simulation run. After the simulation has run for a while, you may see a warning dialog indicating that the maximum time has been reached. To restart the simulation, simply click on the Reset button then click on the Run button in the simulation window.

• SimLoad searches the directories specified in the Models Directory dialog. If the default Models directory has not been installed or has been renamed then no models will be found.



Placing Control Devices

• Select the "primio.clf" library in the Parts palette. Select and place a Clock device to the left of the diagram, as shown.

This device will generate a repeating clock signal that will drive the circuit. The clock parameters can be set by selecting the device and using the Parameters command in the Simulator menu.

• Select and place a Binary Switch device and a Binary Probe device to the left of the diagram, as shown.

• Return to the pointer ( ) tool by clicking on the menu bar.

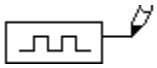
• Click on the switch symbol and notice that it changes state.

These display and control devices are active right on the schematic and will be updated as the simulation progresses.

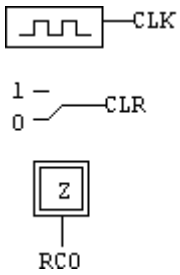
Placing Control Devices (cont'd)

• Using the text (T)tool, click on the end of the pin in the clock device.

• Enter the name "CLK" and press Enter.



This assigns the name CLK to the output signal of the clock device, logically connecting it to the other signals on the schematic that were already named CLK.



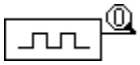
Placing Control Devices (cont'd)

• Apply names "CLR" and "RCO" to the switch and probe devices as shown using the same technique described above.

Notice that the value displayed on the probe changes when the connection by name is registered.

Probing the Schematic

• Select the Signal Probe ( ) tool from the tool palette.

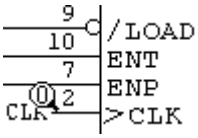


• Click and hold the probe tip on the output of the Clock device.

You will see the state of the probe flicker back and forth between 1 and 0 as the clock device generates its output transitions.

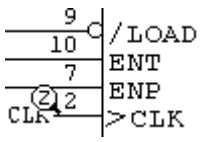
• Release the mouse button.

Probing the Schematic (cont'd)



• Click and hold the probe tip at the end of the CLK input pin on the counter device.

The clock signal is also present at this point due to the connection by name between the two signal segments.

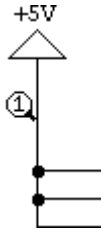


Probing the Schematic (cont'd)

• Click and hold the probe tip on the CLK input pin on the counter device, closer to the body of the device, as shown.

The probe indicates a "Z" (high impedance) value. When the probe is clicked on a pin close to the device body, the drive value on that pin is displayed, instead of the overall signal value. In this case, this is an input pin and its drive value is high impedance. This feature can be used to isolate problems of conflicts created by multiple drives on a single line.

Power and Ground Connections



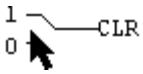
• Still using the probe tool, click and hold on the +5V connections to the counter device, as shown. If this line indicates a "Z" value (high impedance), then it will be necessary to inject a high value.

Some earlier versions of DesignWorks Schematic did not place a simulation value on signals that were connected to power or ground connectors. The power symbols in all current libraries will place the correct simulation value on the attached signal.

• If the probe indicated a "Z" value above, then click and hold the probe cursor on the power signal line. While still holding the mouse button, press the "1" key. You will see the probe change to the 1 value indicating that the signal has changed state. Release the mouse button.

• Repeat this procedure on the ground line, except this time press the "0" key (if it is not already at the 0 level).

This procedure only needs to be done on any one ground line, even if there are many ground symbols in the circuit. All like symbols are effectively connected together for simulation purposes.



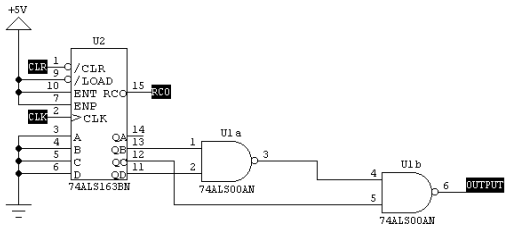
Controlling the Simulation

• Using the pointer ( ) tool, place the switch device in the "0" state, then return it to the "1" state.

This should clear the counter device so that we now see a "0" on the RCO probe, occasionally flicking to the "1" state as the counter passes its terminal count.

If the RCO line remains in an X (Don't Know) or Z (high impedance) state, recheck the signal names and connections. You can also use the Probe tool and the Pin List command (in the signal pop-up menu) to check signal connectivity.

Note: Switch devices normally just change state when you click on them and don't become selected. To select a switch device (e.g. to move it), hold the Shift key while clicking on it.



Displaying the Timing Window

In order to display a signal in the timing window, it must be named. Although all signals are given default names when they are created, it is best to add a meaningful name to signals that will be displayed in the schematic.

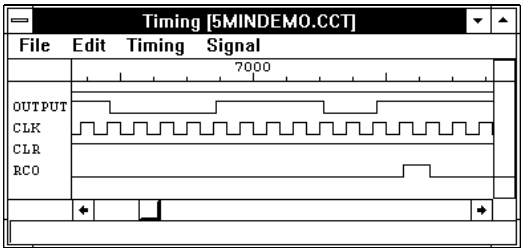
• Using the text (T) tool, apply the name OUTPUT to the signal emerging from the rightmost NAND gate.

• Return to the pointer ( ) tool.

• Holding the SHIFT key pressed, click on the OUTPUT, CLK, CLR and RCO lines to select them.

When signals are connected by name (e.g. CLR in this circuit), you can select any or all connected segments for this operation.

Displaying the Timing Window (cont'd)

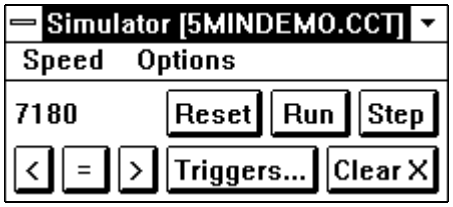


- **Select Timing from the Tools menu in the DesignWorks window.**

This will display an empty timing window associated with the current design and also the Simulator window.

- **Select the Add to Timing command from the Timing menu in the Schematic window.**

This will add any signals that are selected in the schematic to the Timing window. The selected signals will now scroll from right to left as the simulation progresses.



Using the Simulator Window

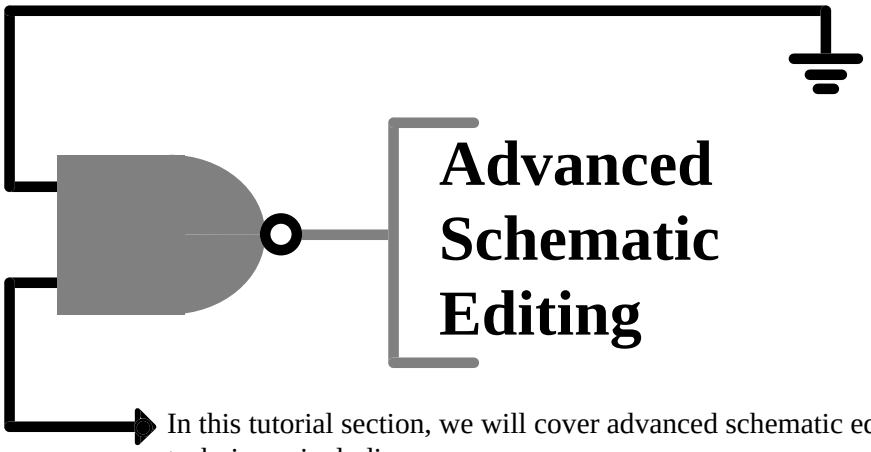
This window contains function to control both the Simulator and Timing window.

- The status area in the top left corner of the window indicates the current simulation time
- The Reset button resets the simulation time to zero, sets up initial values (if any) and clears both the Timing and Test Vector tools.
- The Run button starts the simulator at maximum speed.
- The Step button is used to single step the simulator.
- The Clear X button attempts to remove Don't Know values from the circuit by clearing storage devices and setting device outputs to known values.
- The Triggers button displays the Trigger dialog.
- The <, = and > buttons can be used to zoom the Timing window.

These items will be described later in this manual.

This completes the tutorial section “The 5-Minute Simulation”.

- If you are using the full DesignWorks package, then you may wish to use the Save As command from the File menu to save the completed example at this point. The original file will be referred to in later sections.



Advanced Schematic Editing

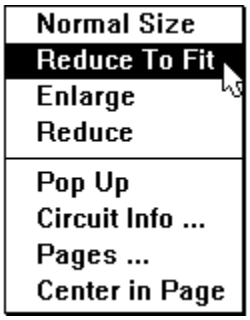
In this tutorial section, we will cover advanced schematic editing techniques including:

- More Editing Techniques
- Pop-Up Menus
- Busses and Breakouts
- Multi-Page Schematics
- Sheet Size Settings
- Text Notations and Grapnics
- Creating Attribute Fields
- Device Packaging

Starting the Program

• If it is not already running, double-click on the DesignWorks icon to start the program.

• Use the Open Design command to open the demonstration file "5mindemo.cct" provided in the Demo directory OR create it using the instructions given earlier in this manual.

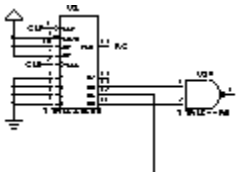


Navigating Around the Schematic

• Press the right mouse button (Right-click) in an empty area of the schematic (i.e. not on a device or signal line).

• In the pop-up menu that appears, select the command Reduce to Fit.

The screen display will be zoomed out to fit the entire schematic in the window. Right-clicking in the schematic displays a pop-up menu containing short-cut editing commands. Right-clicking on a device, signal, pin or attribute field will display a special menu for each type of object.



Navigating Around the Schematic (cont'd)

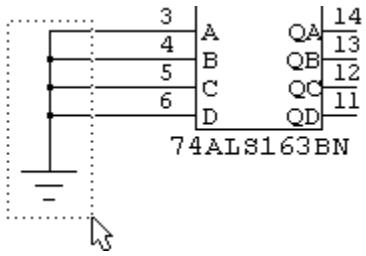
• Click on the magnify (🔍) tool in the tool palette and then click near the A B C D input pins of the 163 counter.

Clicking the magnifying glass tool zooms in on that part of the schematic. Some less obvious uses of this tool are:

• Clicking and dragging down and right causes the display to zoom so that the area swept over just fits in the window.

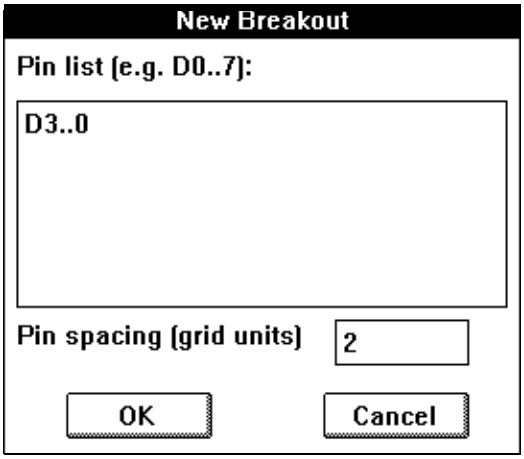
• Clicking and dragging up and to the left a small amount causes the display to zoom out one step.

• Clicking and dragging up and to the left a large amount (more than 1/2 the screen) causes the display to do a Reduce to Fit.



Deleting a Group of Objects

- **Using the pointer ( ) tool, click and drag from above and to the left of the ground symbol to below and right of it.**
- **Make sure that the ground symbol itself and the attached signal line are highlighted and no other items.**
- **Press the Backspace key to remove these items.**

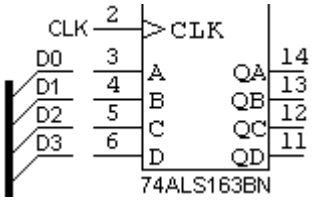


Creating a Bus

- **Select the New Breakout command from the Options menu. In the signal list area of this dialog, enter "D3..0".**
- **Click on the OK button.**

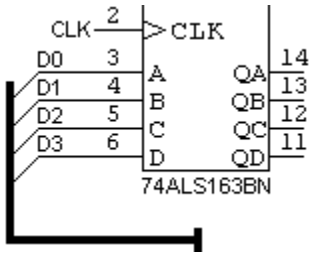
We used sequentially numbered signals in this case, but any collection of names can be used, for example "CLK CLR SIZ0 SIZ1". "0..3" places the highest numbered signal at the top, "3..0" places it at the bottom.

Creating a Bus (cont'd)



- **Place the "breakout" symbol adjacent to the 163 device, as shown. Use the arrow keys or tool palette if necessary to orient the breakout symbol.**
- **If not done already, connect the 4 breakout pins to the inputs of the 163 device.**

A "breakout" is a pseudo-device symbol that ties any collection of signal lines into a single bus line. You can extend a bus line away from either end of the "spine" of the breakout symbol.



Creating a Bus (cont'd)

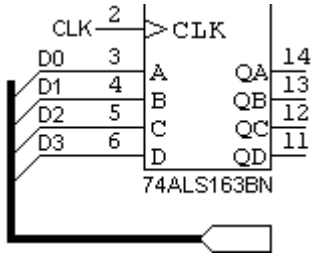
• Using the pointer ( ) tool, click and hold exactly at the lower end of the "backbone" of the breakout symbol.

• Drag down and right from this point, then release the mouse button. This will have created a bus line as shown.

• Right-click on the bus line. In the pop-up menu, select the Signal Info command.

When the Signal Info command is selected for a bus, a list of the internal signals is displayed.

• Click on the OK button.



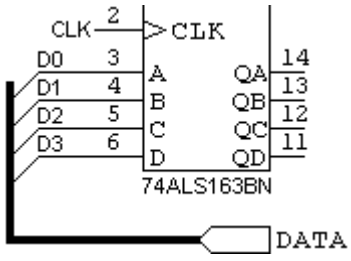
Creating a Bus (cont'd)

• In the Parts palette, select a "Page Conn (Bus)" device in the "pseudo.clf" library.

• Place this symbol as shown so that it connects to the bus that was created above.

The Page Connector symbol indicates that this bus will be connected to other busses with the same name on other pages of the schematic. Without this symbol, connections by name occur only within a single page.

Creating a Bus (cont'd)



• Select the text (T) tool in the tool palette.

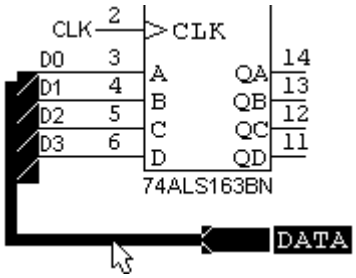
• Click and hold on the Page Connector symbol.

• Still holding the mouse button, move to a point just right of the symbol, then release the button.

• Enter the name "DATA" then press the Enter key.

We have now named the bus "DATA". This has no effect on the names of the internal signals, which still retain the names that were assigned in the New Breakout dialog.

Using the Clipboard



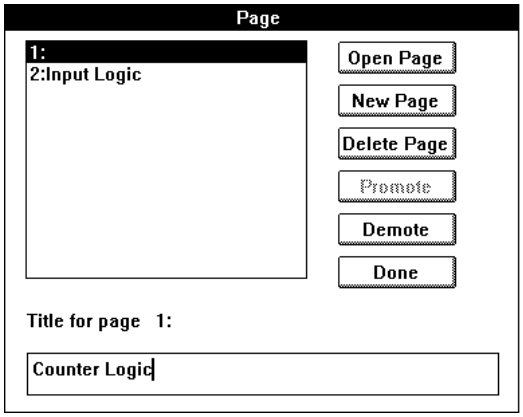
• Return to the pointer ( ) tool and click in an unused area of the schematic to ensure that no items are selected.

• Click on the breakout symbol (i.e. on the diagonal line area in the middle of the symbol), to select it.

• While holding the Shift key, click on the bus line and then on the Page Connector symbol. All three of these items should now be highlighted.

Using the Shift key, you can select any collection of items on one page. These items can then be operated on in subsequent menu commands.

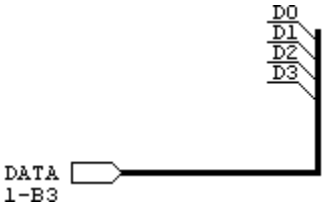
• Select the Copy command from the Edit menu.



Adding a Page

- **Select the Pages command from the Drawing menu.**
- **Click on the New Page button.**
- **Enter the title "Input Logic".**
- **Click on the item "1" in the page list and enter the title "Counter Logic".**
- **Click on the Done button.**

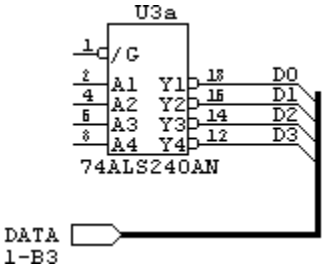
We have now added a second page to the circuit, which can be edited in its own window. The second page is still logically part of the same circuit and will be stored in the same file. A single circuit can have up to 1000 pages.



Adding a Page (cont'd)

- **Select the Paste command from the Edit menu. A flickering image of the bus lines copied from the first page will now appear.**
- **Using the arrow keys, orient this entire group so that the Page Connector is on the left and the breakout is on the right.**
- **Click in the middle of the page to place the circuit segment.**

You will notice that a new notation appears next to the Page Connector symbol. This is an automatic page reference which indicates the page and grid position of other page connectors attached by name to this one.

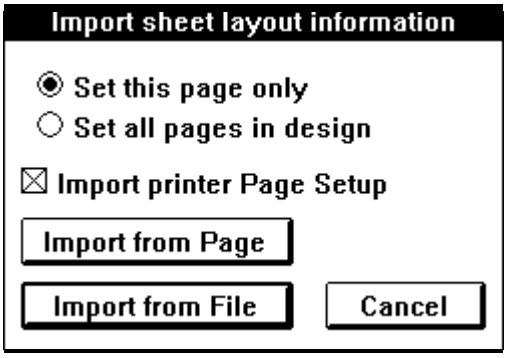


Adding a Page (cont'd)

- **Select a 74ALS240 device from the "74als_c.clf" library and place it so the its outputs connect with the breakout.**
- **Drag this new device away from the breakout to expose some signal lines between the two.**
- **Right-click on one of these lines.**
- **In the pop-up menu, select the Pin List command.**

The Pin List dialog will now indicate that the pin on the 240 device is connected via the bus and page connector to the 163 device on Page 1.

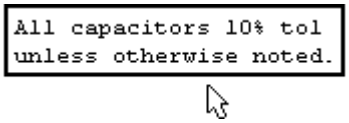
- **Double-click on a pin on U2 to return to the first page.**



Setting Sheet Size

- **Select the Import Sheet Info command from the Drawing menu.**
- **Click on the Set all pages in design box.**
- **Click on the Import from File button.**
- **Locate and open the file "a_bsize.cct" (ANSI B-Size Template) in the Template directory.**

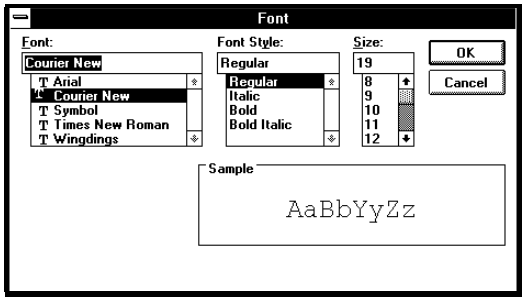
You will now see that both pages in our design will be updated with new sheet size settings and border graphics. A "template" file is really just a normal design file that had custom sheet size settings and border graphics placed in it. You can import sheet info from any design file.



Adding Text Notations

- **Move to an unused corner of the schematic page.**
- **Select the text (T) tool in the tool palette.**
- **Click in an open area of the schematic (i.e. not on an existing device, signal or text item). You will see a text entry rectangle.**
- **Enter "All capacitors 10% tol unless otherwise noted", or any other notation that suits you. Carriage returns can be used in text notations, if desired.**
- **Click outside the text entry rectangle.**

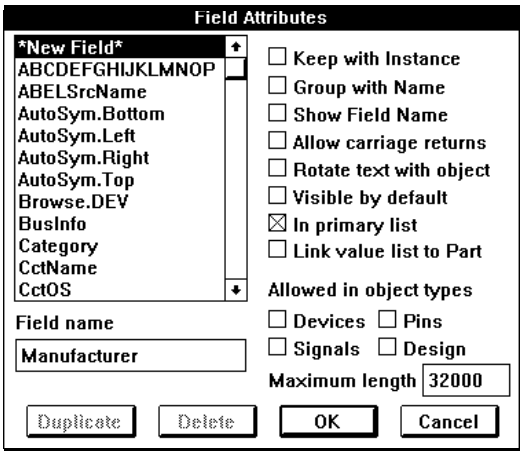
Text notations created in this fashion are stored with the circuit, but are not associated with any device or signal and will never appear in a netlist.



Adding Text Notations (cont'd)

- **Right-click on the text item that was just created.**
- **Select the Draw Frame option.**
- **Click on the Font Specs button.**
- **Use the controls in this dialog to set any desired text style.**
- **Click on the OK button in both dialogs to return to the schematic.**

Text style can be set individually for random text notations such as this one. Other forms of text such as attribute and pin numbers have global text style settings, but cannot be set individually. See the Design Preferences command from the Drawing menu.

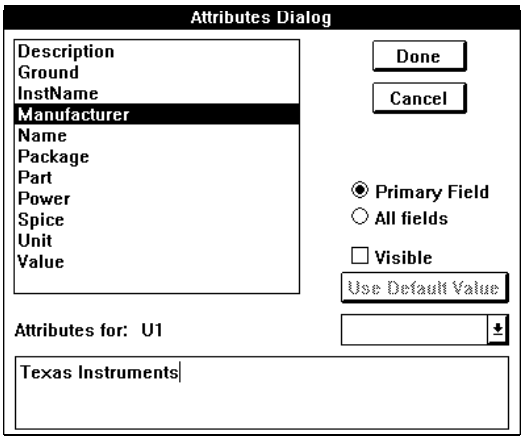


Creating Attribute Fields

- **Select the Define Attribute Fields command from the Options menu.**
- **Enter the name "Manufacturer" in the Field Name box.**
- **Click on the Devices box under "Allowed in object types".**
- **Click on the OK button.**

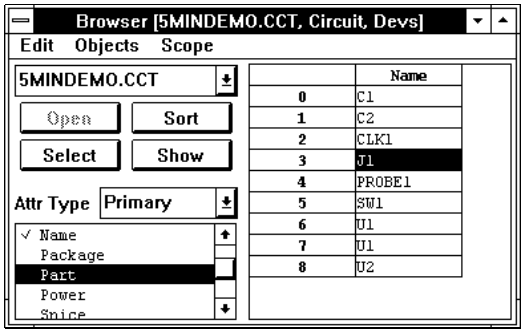
You have now defined a new attribute field that will be associated with devices. A separate value can be entered for each device in your design. The other options in this dialog determine how the value is stored and displayed on the schematic.

Creating Attribute Fields (cont'd)



- **Right-click on any device in the schematic.**
- **In the pop-up menu, select the Attributes command.**
- **Enter a value for the Manufacturer field in the text box.**
- **Click on the Done button.**
- **Repeat this for each device.**

Attribute values can be entered for devices, signals, pins and for the design itself. These values can be displayed on the schematic and extracted in netlists and bills of materials for external use.



Using the Browser Tool

• Click in an unused area of the schematic to ensure that no devices or signals are selected.

• Select Browser from the Tools menu in the DesignWorks window. The Browser tool provides a spreadsheet view of the schematic.

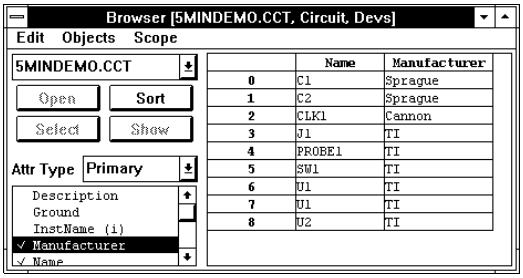
• Click on the Sort button in the Browser palette.

The Browser displays the selected type of object in a spreadsheet format. This allows you to easily locate items and edit attributes without having to search for them on the schematic sheet.

• Click on any device name in the list and click on the Show button.

Notice that the schematic sheet is scrolled to display the selected device. The Browser can also view Signals or Pins (see the Objects menu).

Using the Browser Tool (cont'd)



• Click on the Attr Type control and select the Primary attributes.

• In the Attr List Box, double-click on the Manufacturer field, or any other desired field, to add it to the Browser window.

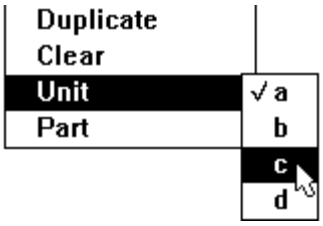
• Double-click on any box in the "Manufacturer" column and entered any desired values.

• Use the Enter key to move down to other cells in the same column.

Changes made to data in the Browser cause the Schematic to be updated immediately. These changes cannot be canceled or undone!

• Close the Browser.

Device Packaging

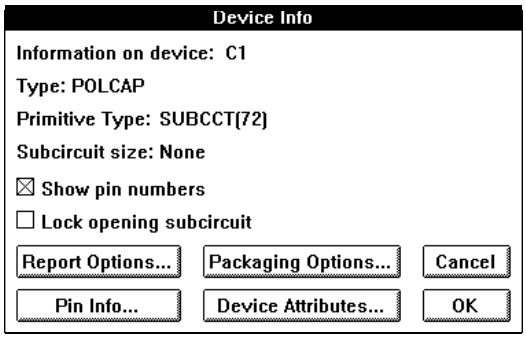


• Right-click on one of the NAND gate devices on page 1.

• Move down to the Unit sub-menu, near the bottom.

• Select Unit "c" in the Unit sub-menu.

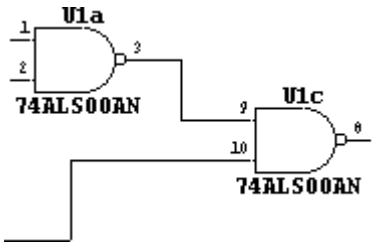
The Unit sub-menu contains a list of all gate units available for this part type. Selecting a different unit will update the pin numbers to correspond.



Device Packaging (cont'd)

- **Right-click on the same device as in the previous section and select the Device Info command.**
- **Click on the Packaging Options button.**
- **Select the "Lock and check package and unit" option.**
- **Click on the OK button in both dialogs.**

The Packager has now been instructed to keep this device name unchanged but check it for conflicts in future packaging operations.



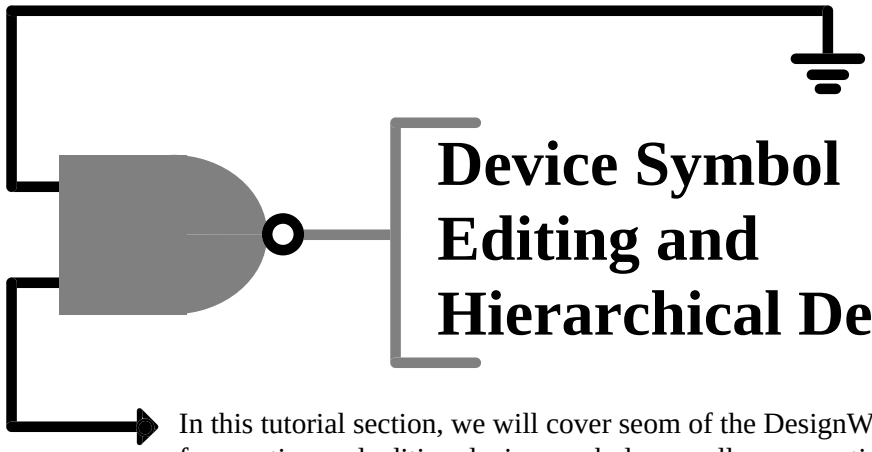
Device Packaging (cont'd)

- **Select the Default Prefix command from the Packaging sub-menu of the Options menu.**
- **Enter the prefix "XX" and click on the OK button.**
- **Select the Repackage Design command from the Packaging sub-menu of the Options menu.**
- **Click on the OK button in the confirmation dialog.**

Notice that new names have now been assigned to all devices except the one that we marked as "Lock and Check". Names are assigned starting in the "A1" grid of the schematic, working toward the opposite corner.

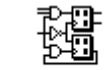
This completes the tutorial section “Advanced Schematic Editing”.

- The remaining tutorials deal with specific areas of the program and do not make further reference to this file.



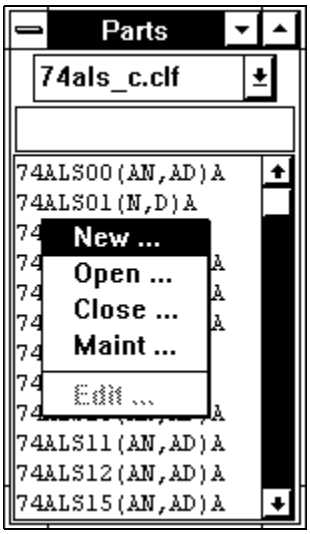
Device Symbol Editing and Hierarchical Design

In this tutorial section, we will cover seom of the DesignWorks features for creating and editing device symbols as well as assocating internal circuits with them.



Starting the Program

• If it is not already running, double-click on the DesignWorks icon to start the program.

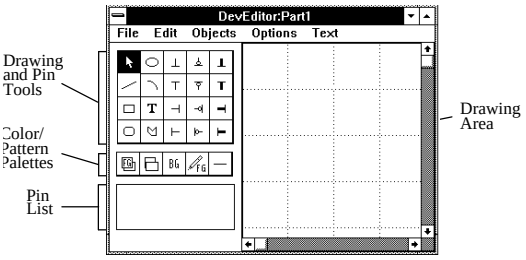


Creating a New Library

• Right-click on the Parts palette's parts list and select the New command from the pop-up menu.

• Create a new library called "MyLib.dlf" in the Libs directory.

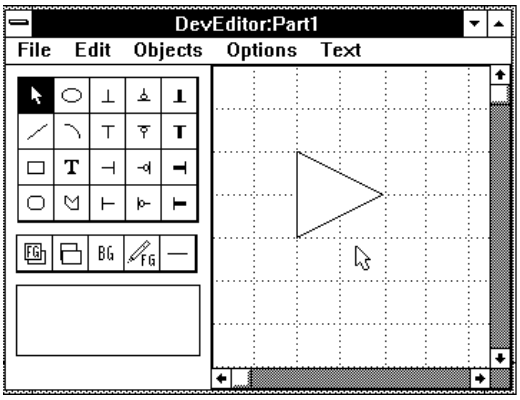
Device library files hold collections of part symbols along with associated pin function information, default attribute values and external circuit references. A single library can contain from one to thousands of part definitions, to suit your needs.



Creating a Device Symbol

• Select DevEditor from the Tools menu in the DesignWorks window.

The DevEditor window contains a drawing area for your symbol, a tool palette and a pin list. The tool palette includes standard drawing tools plus special items for normal, inverted and bus pin placement.



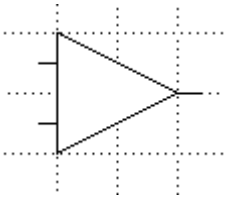
Creating a Device Symbol (cont'd)

• Select the Grids command from the Options menu.

• Set the Pin Grid Spacing to 1 and click on the Set button.

• Click on the polygon (⋀) tool in the tool palette.

• Draw a symbol similar to the one shown (Note: double click on the last point to terminate polygon drawing).



Creating a Device Symbol (cont'd)

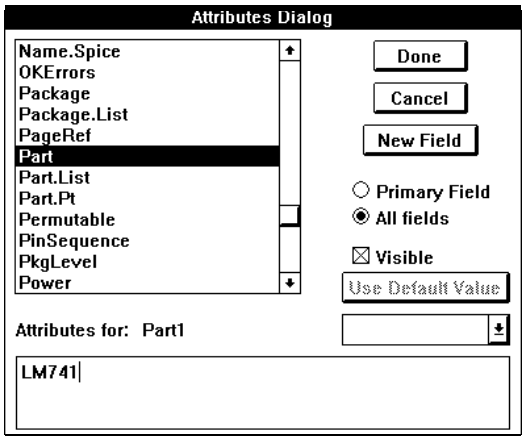
• Select the (⊢) pin tool.

• Place input pins on the symbol by clicking at the positions shown.

• Select the (⊢) pin tool.

• Place an output pin as shown.

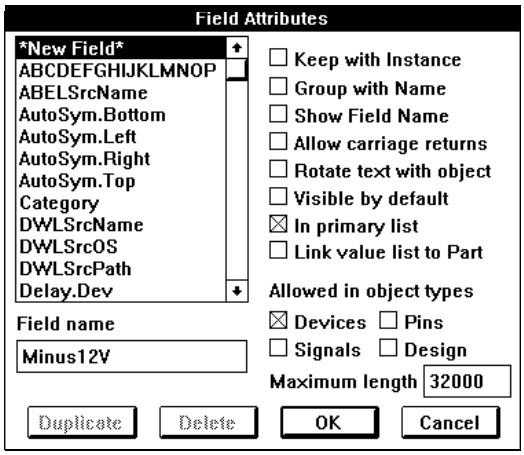
Note: The crossbar portion of the T pin tool only appears during placement and dragging for alignment purposes.



Setting Default Part Attributes

- **Return to the pointer ( ) tool.**
- **Select the Part Attributes command from the Options menu. (Note: there will be no attributes in the list if there is no active design).**
- **Select the Part field in the list.**
- **Enter the value "LM741".**
- **Select the Package field in the list.**
- **Enter the value "NAT8DPN" or other package code.**

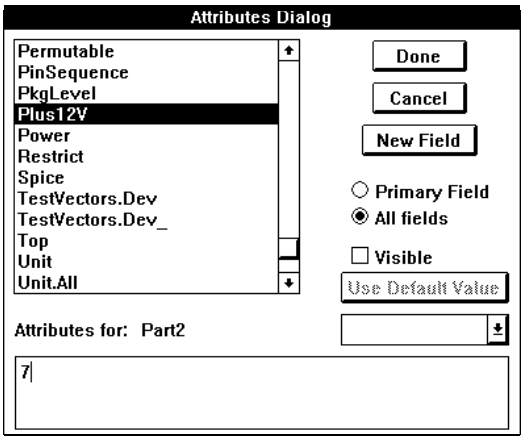
These attribute values will appear as the defaults when this part is used on a schematic. If desired, these values can be overridden for each individual device.



Setting Default Part Attributes (cont'd)

- **Click on the New Field button in the attributes dialog.**
- **Enter the field name "Plus12V" then press the Tab key to terminate this value.**
- **Select the "New Field" item at the top of the list again.**
- **Enter the field name "Minus12V".**
- **Click on the OK button.**

If you create multiple devices in succession, you only need to perform the "New Field" operation once since the DevEditor keeps the same field list for all devices.

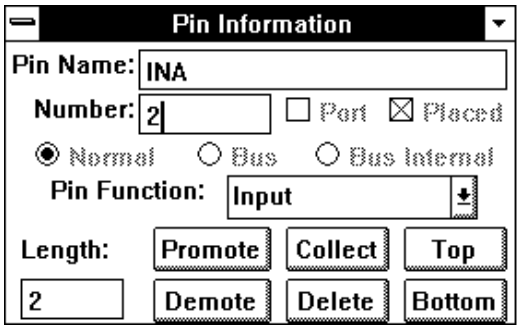


Setting Default Part Attributes (cont'd)

- **Enter the value "4" for the new Minus12V field.**
- **Enter the value "7" for the "Plus12V" field.**

These entries will determine the default power connections for this device in a netlist.

- **Click on the Done button to close the attributes dialog.**



Entering Pin Names and Numbers

• Double-click on the PIN1 item in the pin list.

• In the Pin Info palette that appears, enter the pin name "INA" then press the Enter key to move to the next pin in the list.

• Enter the pin name "INB" then press the Enter key to move to the last pin in the list.

• Enter the pin name "OUT" then press the Enter key to move to the first pin in the list.

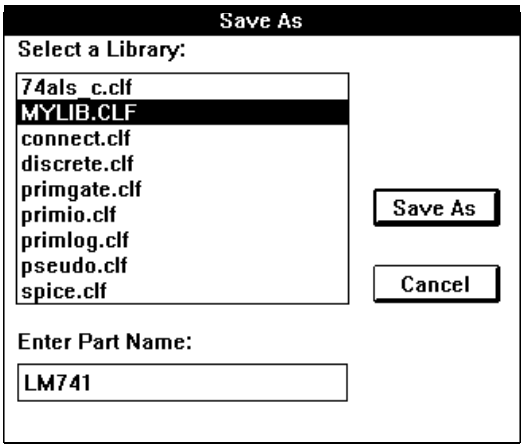
• Enter the pin number 2 then press the Enter key to move to the next pin in the list.

• Enter the pin number 3 then press the Enter key to move to the last pin in the list.

• Enter the pin number 6 then select Output from the Pin Function pulldown box.

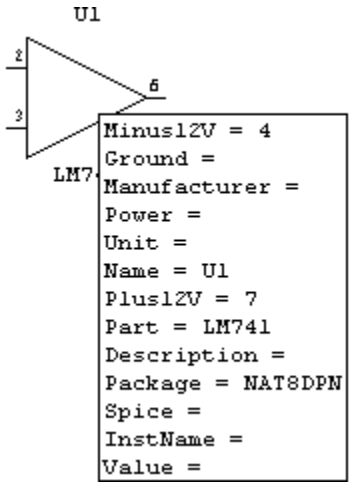
• Press the Enter key to complete the last pin, then close the Pin Info dialog by double clicking on the menu in its top left corner.

We have now entered default values for the pin numbers that will appear in a netlist. These can be edited on the schematic for individual pins, if desired.



Saving and Using the Part

- **Select the Save Part As command from the File menu.**
- **Enter the part name "LM741" or any other desired name.**
- **Click on the "MyLib.clf" library in the list to select a destination and press "Save As".**
- **Close the DevEditor.**

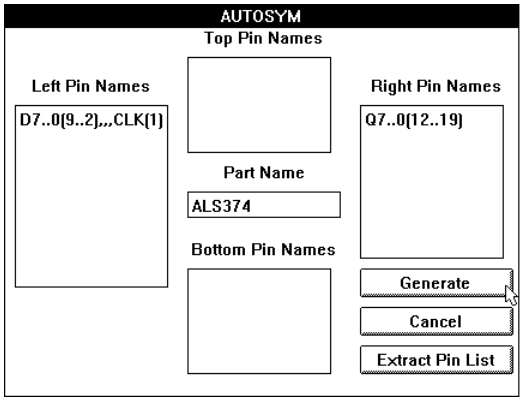


Saving and Using the Part (cont'd)

- **If it is not already selected, select the "MyLib.clf" library in the drop-down library list in the Parts palette.**
- **Double-click on the newly-created part and place one in the schematic.**

Note: A warning dialog will be displayed indicating that new attribute fields are being defined.

- **Select the Attribute Probe (?) tool in the schematic tool palette.**
- **Click on the new device to verify that the default attribute values appear.**



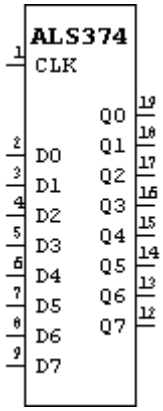
Auto-Creating a Symbol

For standard types of rectangular symbols, the Auto Create feature will generate a symbol for you in seconds.

- **Select DevEditor from the Tools menu in the DesignWorks window.**
- **Select the Autocreate Symbol command from the Options menu.**
- **In the Name box, enter "ALS374", or any other desired symbol name.**
- **In the "Left Pins" box, enter the text "D7..0(9..2),,,CLK(1)".**

"D7..0" will generate a set of 8 pins named D7, D6, etc. "(9..2)" are the corresponding pin numbers. The three commas indicate that we want extra space between these pins. "CLK(1)" creates a single pin called CLK with pin number 1. The pin numbers can be omitted, if desired.

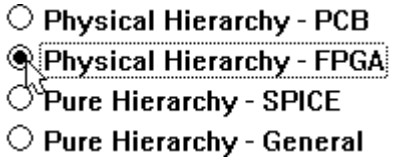
- **In the "Right Pins" box, enter the text "Q7..0(12..19)".**
- **Click on the Generate button.**



Auto-Creating a Symbol (cont'd)

The auto-generated symbol should now display the pins and pin numbers entered above. These items can be edited using the drawing tools and Pin Info dialog, if desired.

- **Select the Save Part As item in the file menu and save the new part to the "MyLib.clf" library.**
- **Close the DevEditor window.**



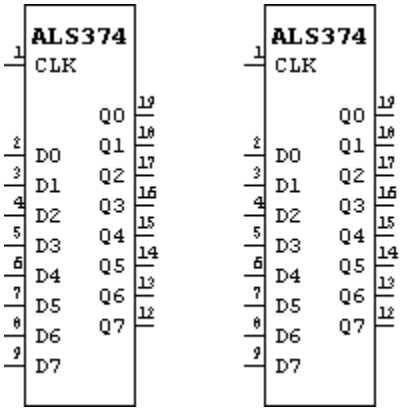
Creating a Hierarchical Block

• Select the New Design command from the File menu in the DesignWorks window.

• When the Design Mode dialog appears, Select the Physical Hierarchy - FPGA mode.

• Click on the New Design button.

We have now selected Physical Hierarchy mode, which will allow us to create nested circuit blocks inside device symbols.

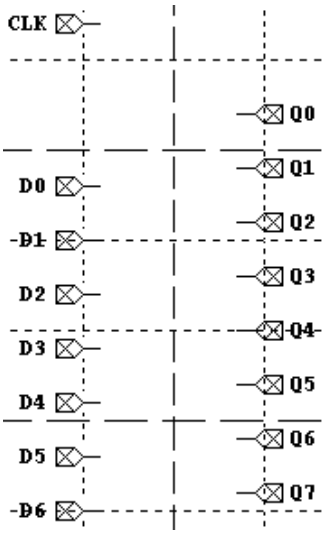


Creating a Hierarchical Block (cont'd)

• In the Parts palette, double-click on the ALS374 device that was just created.

• Place two of these devices on the schematic, as shown.

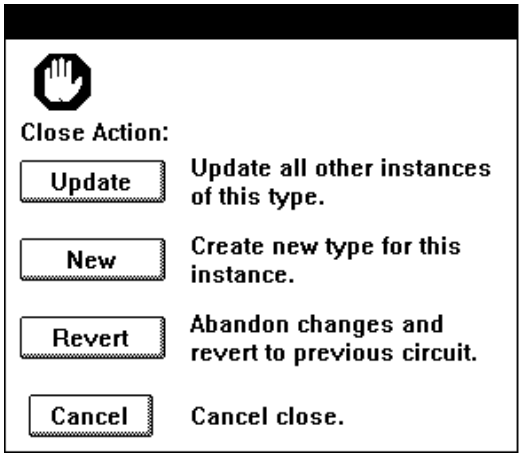
When new symbols are made in the DevEditor, they are set by default to be "Sub-Circuit" devices, meaning that an internal circuit can be created in them, even if none is provided initially.



Creating a Hierarchical Block (cont'd)

- **Double-click on either of the ALS374 devices that were just placed.**
- **Click on the OK button in the warning dialog to create an internal circuit.**

A new window will now appear showing the internal circuit for this block. When a new internal circuit is created, "port connector" symbols are automatically laid out to match the pins on the parent symbol. Any signal connection made to a port connector becomes logically connected to the pin with the same name on the parent symbol.



Creating a Hierarchical Block (cont'd)

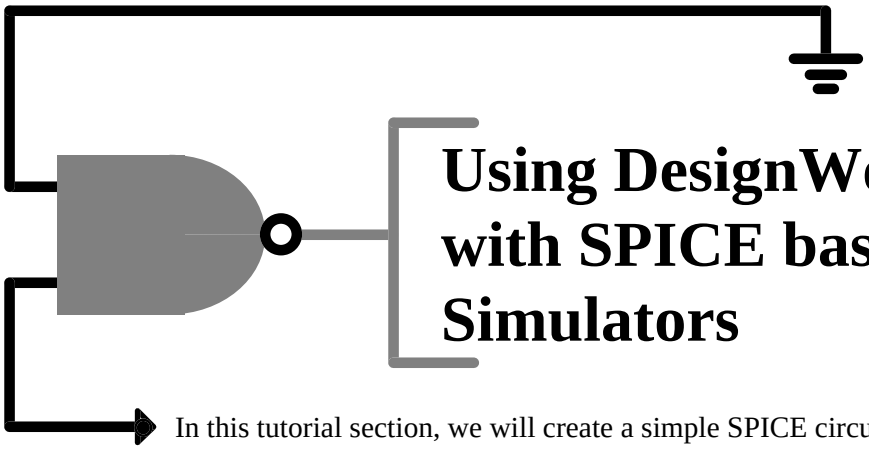
- **Close the internal circuit window.**
- **A dialog will appear allowing you to select the appropriate action in updating the part definition. Click on the Update button.**

The "Update" option will cause the definition of all devices of the same type to be updated throughout the design. Double-clicking on any other device of the same type will now reveal the same internal circuit.

Note: Unless you are an experienced user of hierarchical design concepts, please refer the chapter "Before Starting a Major Design" in the DesignWorks Reference Manual before using these features.

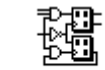
This completes the tutorial section “Device Symbol Editing and Hierarchical Design”.

- More information on hierarchical design features is found in Appendix A.



Using DesignWorks with SPICE based Simulators

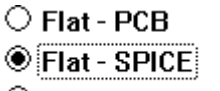
In this tutorial section, we will create a simple SPICE circuit and write out the complete netlist. You can then try out this netlist with your SPICE package.



Starting the Program

• If it is not already running, double-click on the DesignWorks icon to start the program.

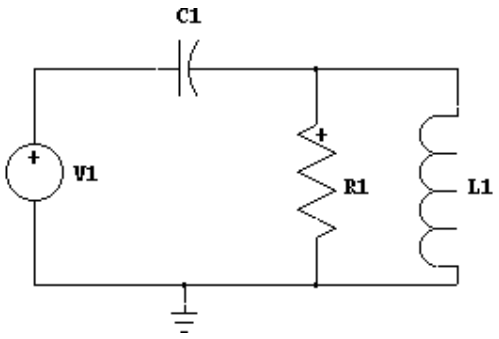
Creating a SPICE Design



• When the Design Mode dialog appears, Select the "Flat - SPICE" mode.

• Click on the New Design button.

This mode enables an option that auto-names devices using a SPICE prefix supplied in the library. In the SPICE library provided with DesignWorks, this field contains the standard prefixes for SPICE models.

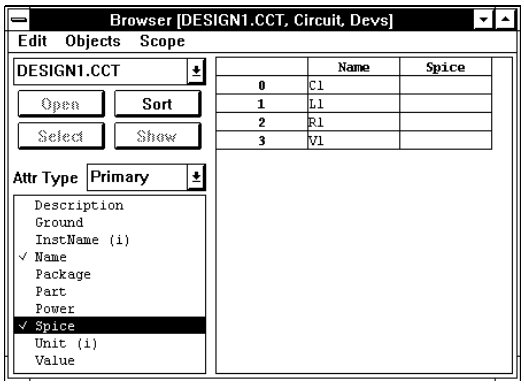


Placing SPICE Devices

• Select the "spice.clf" library in the library selection list in the Parts palette.

• Using the devices Ind Volt. Src, SPICE Ground, SPICE Res, SPICE Cap and SPICE Ind, create the circuit shown at left.

Some of the passive components in this library, such as the SPICE resistor, are marked to ensure consistent polarity for current-measuring purposes.



Entering SPICE parameters

• Click in an unused area of the schematic to ensure that no devices or signals are selected.

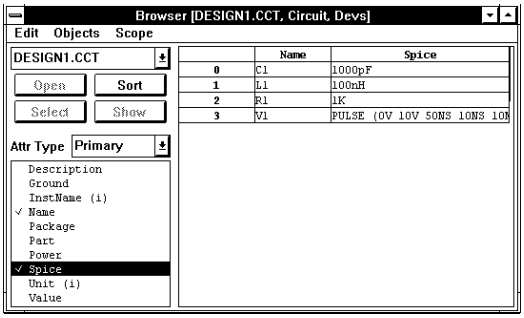
• Select Browser from the Tools menu in the DesignWorks window.

• Click on the Sort button in the Browser palette.

• Click on the Attr Type control and select the Primary attributes.

• In the Attr List Box, double-click on the Spice field to add it to the Browser window.

All text entered in the Spice attribute will be included in the netlist for with the associated device.



Entering SPICE parameters (cont'd)

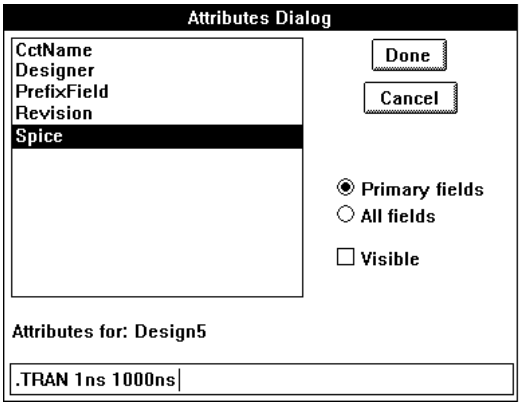
- **Click in the cell under SPICE adjacent to the device C1 in the Name list.**
- **Enter the value "1000pF"**
- **Enter values for the remaining devices as follows:**

  L1 100nH

  R1 1K

  V1 PULSE(0V 10V 50NS 10NS 10NS 100NS 1US)

- **Press the Enter key to ensure that the last value to be sure the schematic is updated.**
- **Close the Browser.**

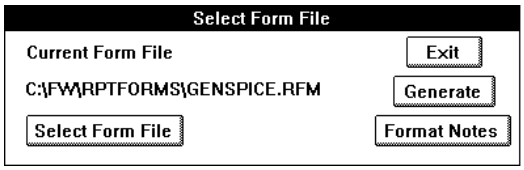


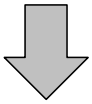
Entering SPICE Parameters (cont'd)

- **Select the command Set Design Attributes in the Options menu.**
- **Select the Spice field in the list.**
- **Enter the text ".TRAN 1ns 1000ns". If you are using PSpice, you may wish to press the Enter key and enter a ".PROBE" line to generate output for the Probe display program.**

Any text entered in the design's Spice field will appear at the beginning of the SPICE netlist. This can be used to enter SPICE commands, model definitions, etc. Multiple lines can be entered if desired using the Enter key. You can also use the Ctrl-V (paste) to paste larger numbers of lines into this box.

- **Click on the Done button to close the attributes dialog.**





```
Design2   Thursday, October 22, 1993   11:52 AM
.TRAN 1ns 1000ns
C1  SIG1 SIG4 1000pF
L1  SIG4 0 100nH
R1  SIG4 0 1K
V1  SIG1 0 PULSE (0V 10V 50NS 10NS 10NS 100NS 1US)
.END
```

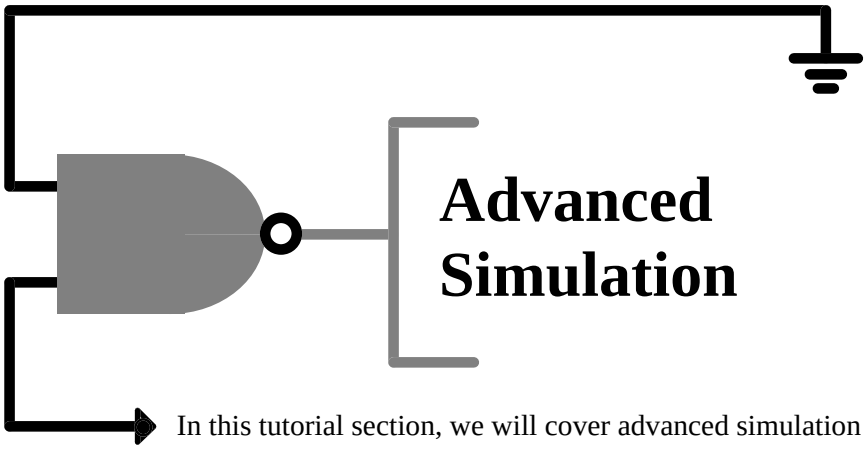
Creating a SPICE Netlist

- **Select Report from the Tools menu in the DesignWorks window.**
- **Click on the Select Form File button.**
- **Locate the file "genspc.rfm" in the Rptforms directory (or, if you have the full DesignWorks package, pick any other SPICE format).**
- **Click on the Generate button.**
- **Select an appropriate output file name and click on the Save button.**

The netlist file just created can now be fed directly to your simulator.

This completes the tutorial section “Using DesignWorks with SPICE-based Simulators”.

- DesignWorks can also directly create hierarchical SPICE netlists with .SUBCKT definitions. Hierarchical block symbols can be nested to any desired depth.



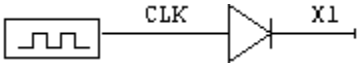
Advanced Simulation

In this tutorial section, we will cover advanced simulation techniques including:

- Setting clocks and delay parameters
- Drive levels and stuck values
- Bidirectional switches
- Displaying grouped traces in hex
- Using triggers to detect glitches

Starting the Program

- **If it is not already running, double-click on the DesignWorks icon to start the program.**
- **When the Design Mode dialog appears, Select the "Flat - General" mode.**
- **Click on the New Design button.**

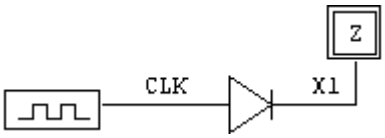


Using Primitive Devices

• Create the circuit shown at left using the "Clock" clock generator device and "Buffer-1 O.C." open-collector buffer device, both in the “primlog.clf” library.

Primitive devices are symbols which have a built-in simulation model in DesignWorks. The symbols included in the Primitive Logic and Primitive Gates libraries are only a sample of the possible combinations. Using the DevEditor tool you can create primitives with a wide range of input and output combinations. Primitive devices do not contain pin numbers and gate packaging information and so are not recommended for board-level designs.

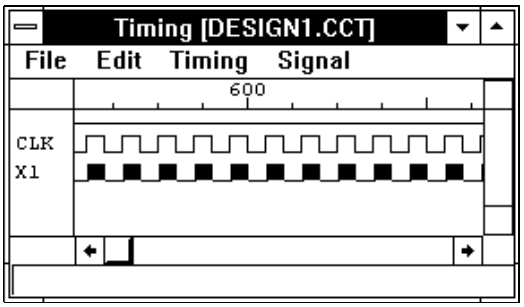
Using Primitive Devices (cont'd)



• Add the Binary Probe device from the “primio.clf” library, as shown.

You will notice the probe is alternating between the 0 and Z states. When the input to the open-collector buffer is high, then output will be undriven and the signal will be in the high-impedance state.

Displaying Waveforms in the Timing Window



• Select Timing from the Tools menu in the DesignWorks window

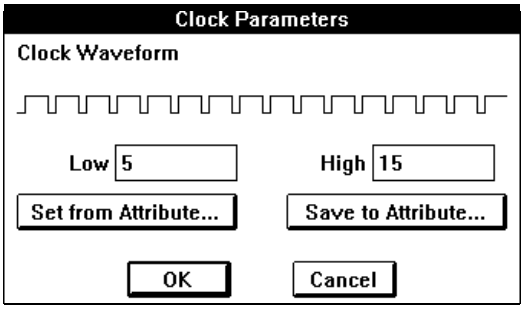
This displays the Timing window.

• Select the Select All command from the Edit menu in the Schematic window.

• Select the Add to Timing command from the Timing menu.

Add to Timing adds all the signals selected in the schematic to the timing window. Notice that the high-impedance value is shown in a different color on signal X1.

Setting Simulation Parameters



• Return to the schematic and select the pointer ( ) tool.

• Click in an unused area of the schematic to ensure that nothing is selected.

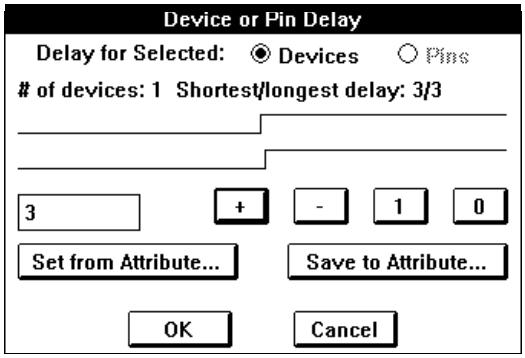
• Click on the Clock device to select it.

• Select the Parameters command from the Simulator menu.

• Enter the value 5 for the Low time and 15 for the High time, then click on the OK button.

Notice that this change has an immediate effect on the timing window. The High and Low times can each be set to any value between 1 and 32767.

Setting Simulation Parameters (cont'd)



• Click on the open-collector buffer device to select it.

• Again, select the Parameters command from the Simulator menu.

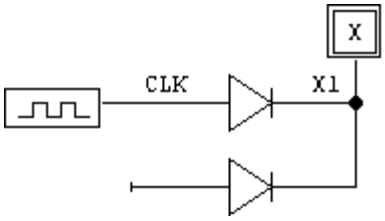
• Use the "+" button to increment the delay value to 3.

• Click on the OK button.

Notice that this immediately affects the timing display for all transitions that occurred after the change was made.

Most primitive devices have a default delay value of 1 unit. This can be changed to any value between 0 and 32767 using this command. The device delay is applied when a value change at any input causes an output to change. Additional delays can be set for individual pins to customize the delays through different signal paths.

Resolving Multiple Drives

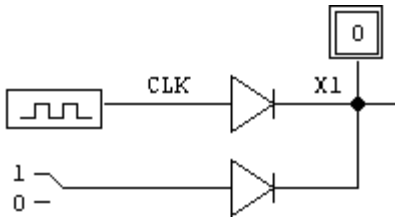


• Using the pointer ( ) tool, click on the buffer device to select it.

• Select the Duplicate command from the Edit menu and place and connect a second buffer as shown.

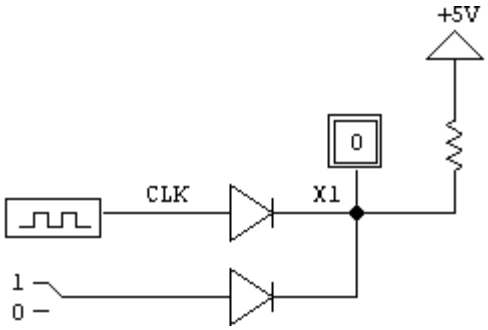
We have now have two device outputs driving a single signal line. Since the input to the lower buffer is not defined, it puts out a value indicating that it might be in either the LOW or HIGHZ states. When the upper buffer puts out a LOW, then the signal value is definitely LOW. When the upper buffer is in the HIGHZ state, the signal value cannot be determined, so the X (Don't Know) value will be displayed on the probe. Notice how this value appears in the timing window.

Resolving Multiple Drives (cont'd)



• Add a Binary Switch (from the "primio.clf" library), as shown.

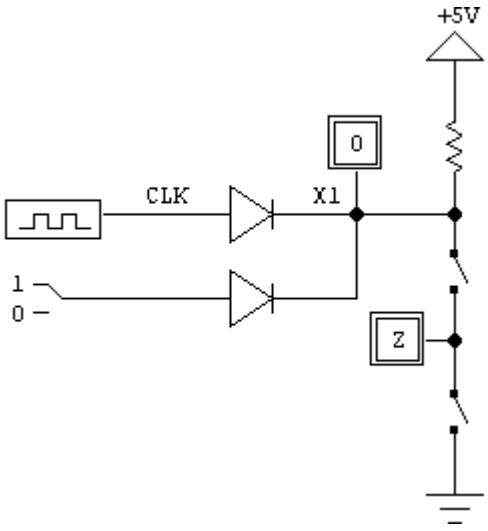
Notice how you can now force a LOW value on the X1 output using the switch device.



Creating a Pullup Resistor

- **Select a Resistor device from the "primlog.clf" library and place it as shown.**
- **Select a +5V symbol from the "pseudo.clf" library and place and wire it as shown.**

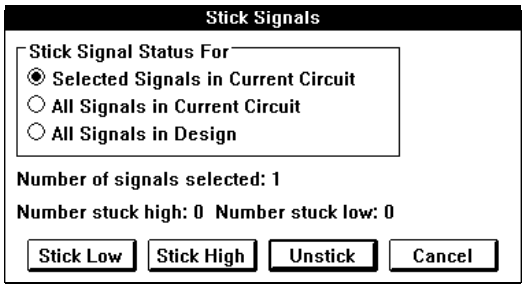
Notice how the X1 signal value will now alternate between 0 and 1, instead of 0 and Z. The +5V symbol generates a continuous 1 value which is fed to the resistor. The resistor device converts this to a "resistive high" value. This means that it can be overridden by another device, but will produce a high value in the absence of any other drive.



Using Bidirectional Switches

- **Select the SPST device from the "primio.clf" library and place two of them as shown.**
- **Select a Ground device from the "pseudo.clf" library and place it as shown.**
- **Place an additional probe at the junction of the two switches, as shown.**
- **Using the pointer ( ) tool, click on each of the SPST switches to change its state and observe the probe values. Note: You must click in the narrow area between the two end dots to change the state of the SPST switch.**

The SPST and SPDT switch devices and the Transmission Gate (XGATE) device are the only *bidirectional* devices in the DesignWorks libraries. When the switch is ON, it acts just as if the two ends were connected and a change at either end will be conducted to the opposite side. (**Note**: This behavior is modified somewhat if a non-zero delay is set.) When the switch is OFF, there is no connection between the two ends.



Stuck Signal Values

• Using the pointer ( ) tool, click on the X1 signal to select it.

• Select the Stick Signals command from Options menu in the Simulator window.

• Click on the Stick High button.

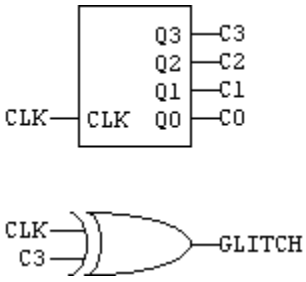
• Click on the switches in the circuit and note that the X1 signal retains a high value.

"Stuck" signal values can be used to set initial values in a circuit, to force power and ground lines to a known value, to check "stuck-at" faults and to isolate parts of a circuit for testing. Once placed in a "stuck" state, a signal will not change value until explicitly unstuck by a user command.

• Select the Stick Signals command again and click on the Unstick button.

The Unstick operation causes the signal to revert to the state resulting from the driving devices attached to it.

Displaying Grouped Signals



• Select a Counter-4 Min. device from the "primlog.clf" library and place it below the other items in the schematic.

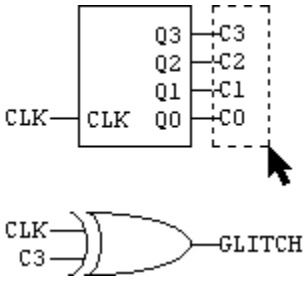
This device is a 4-bit up counter with a positive-edge triggered clock and no other control inputs.

• Select an XOR-2 device from the "primgate.clf" library and place it as shown.

• Using the text (T) tool, name all the pins on these two devices, as shown.

The CLK pins will be connected by name to the existing CLK signal driven by the Clock device.

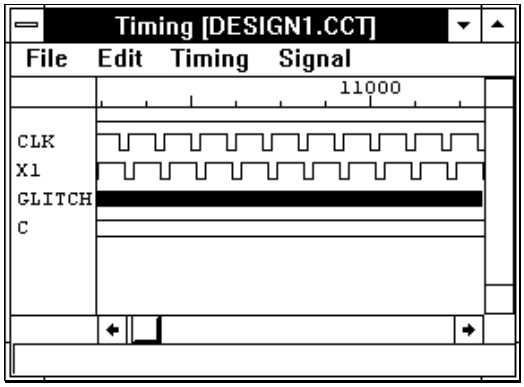
Displaying Grouped Signals (cont'd)



• Using the pointer ( ) tool, click and drag as shown to select signals C0 to C3.

• Select the Add as Group command from the Timing menu.

This command adds the selected signals to the timing display as a single grouped trace, displayed in hexadecimal. Numbered signals will be ordered so that the lowest-numbered signal is the least significant bit of the displayed value. Since the counter is still in an unknown state, no values will be displayed.

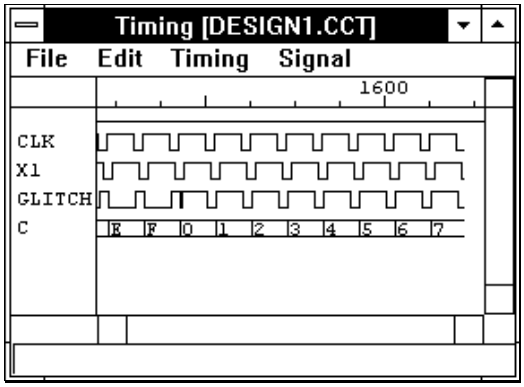


Displaying Grouped Signals (cont'd)

• Click on the GLITCH signal name in the schematic to select it.

• Select the Add to Timing command from the Timing menu.

Clearing the Simulation

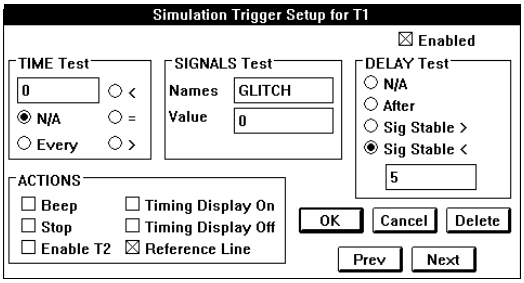


• Click on the Clear X button in the Simulator window.

This will result in the counter device starting to count up from zero.

When storage devices are first placed on the schematic, they take on an "unknown" state. The counter device we placed has no "Clear" input, so there is no circuit operation that will clear to a known value. The Clear Unknowns command clears all storage devices in the design and will attempt to find a defined state for any feedback loops.

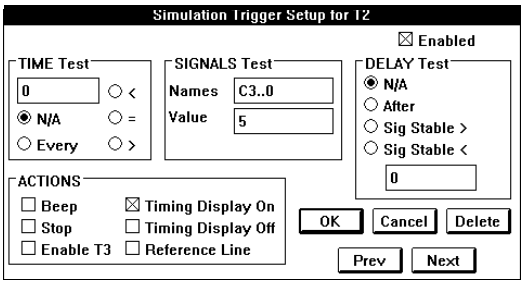
Using Triggers



- **Click on the Triggers button in the Simulator window.**
- **Under SIGNALS Test, enter the name GLITCH in the Names box, exactly as it appears on the schematic, and enter the value 0 in the Values box.**
- **Under DELAY Test, click on the "Sig Stable <" option and enter the value 3 in the Delay box.**
- **Under Actions, click on the "Reference Line" option**
- **Click on the OK button.**

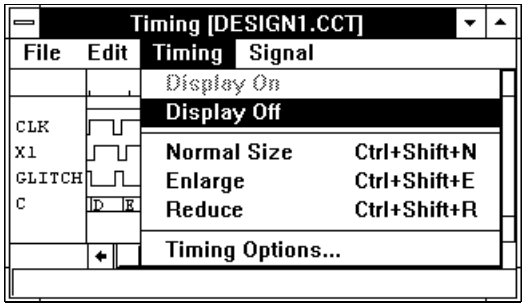
You will now see a reference line appear on the timing window each time the signal GLITCH takes on a 0 value for less than 3 units before changing state.

Using Triggers (cont'd)



- **Again, select the Triggers command.**
- **Click on the Next button, so that the dialog displays "Simulation Trigger Setup for T2".**
- **Under SIGNALS Test, enter the name C3..0 and enter the value 5 in the Values box.**
- **Select the "Timing Display On" option under Actions.**
- **Click on the OK button.**

The notation "C3..0" indicates a numeric sequence of signal names, the first one being the leftmost (most significant) bit of the value. In this case, C3 will be the most significant bit, C2 the next, C1 the next and C0 the least significant.

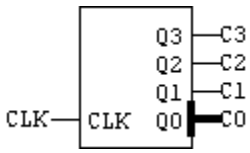


Using Triggers (cont'd)

• Select the Display Off command from the Timing menu in the Timing window.

This disables timing window updates. The simulation continues to advance without displaying any waveforms until the Cx signals reach the value 5. The display is then re-enabled with the event which caused the trigger at the right-hand edge.

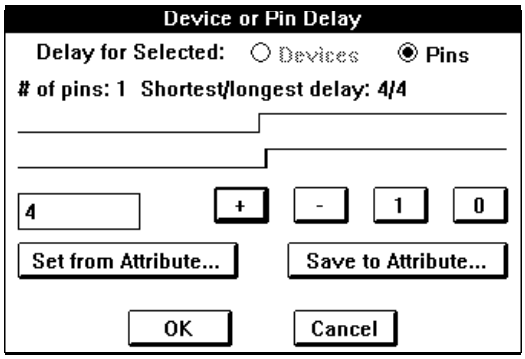
Setting Pin Delays



• Using the pointer ( ) tool, select the Q0 pin on the counter by clicking close to the device body.

Clicking at the end of the pin will select the signal attached to the pin, not the pin itself. When the pin is selected you will see a distinct T shape highlighted.

Setting Pin Delays (cont'd)

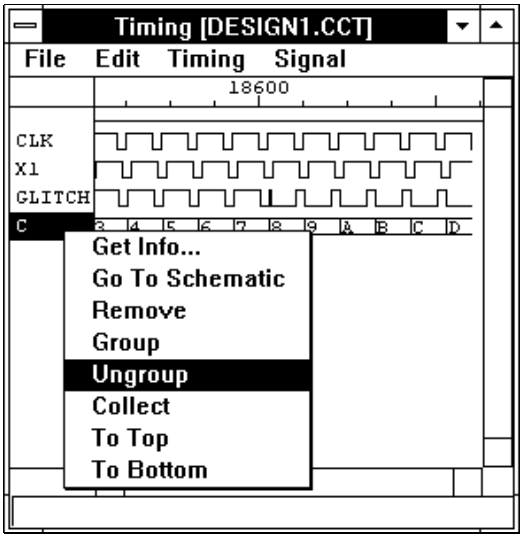


• Select the Parameters command from the Simulator menu.

• Click on the "+" button to increment the pin delay to 4.

• Click on the OK button.

Output transitions on this pin will now be delayed 4 units beyond the other pins on the same device. Notice the effect this has on the grouped trace on the timing window. You may wish to use the Zoom In control ("<>") on the timing control palette to emphasize this delay.



Setting Pin Delays (cont'd)

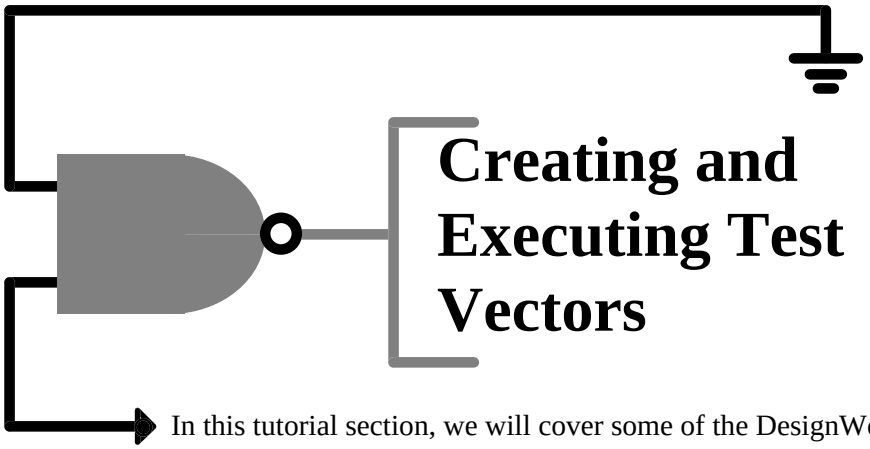
- **Use the right mouse button to select the grouped "C" trace and display the Timing pop-up menu.**

Note: If the window is positioned near the bottom of the screen you may not be able to see all the menu items. If this is the case, reposition the window higher up the screen.

- **Select the Ungroup command from this pop-up menu.**

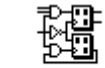
The C3..0 signals will now be displayed in separate traces, allowing you to view the different delay exhibited by the C0 signal.

This completes the tutorial section "Advanced Simulation".



Creating and Executing Test Vectors

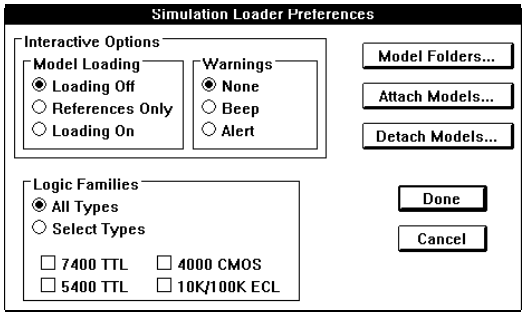
In this tutorial section, we will cover some of the DesignWorks features for creating and executing test vectors as well as using the Test Vector tool for generating test patterns and recording simulation results in text



Starting the Program

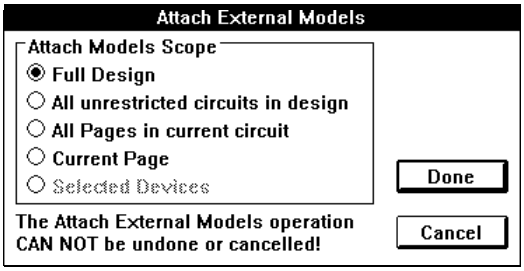
- **If it is not already running, double-click on the DesignWorks icon to start the program.**
- **Use the Open Design command to open the demonstration file "5mindemo.cct" provided in the Demo directory OR create it using the instructions given earlier in this manual.**

Note: For this demonstration to work correctly you must start with a copy of the "5-Minute Schematic" that does not contain the modifications made in the "5-Minute Simulation" tutorial.



Preparing the Design

- **Select SimLoad from the Tools menu in the DesignWorks window.**
- **Click on the Attach Models button.**

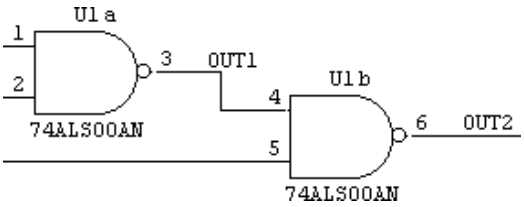


Preparing the Design (cont'd)

- **Click on the Attach button in the Attach External Models dialog.**

The design will now be scanned and models located for the two 74XX devices in this design. A summary dialog will be displayed when the operation is completed.

- **Click on the OK button in the update summary dialog, then click on the Done button in the SimLoad dialog.**

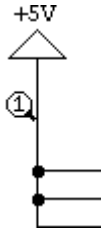


Preparing the Design (cont'd)

- **Apply the names OUT1 and OUT2 to the gate outputs as shown.**

Only named signals can be driven or evaluated in test vectors.

Preparing the Design (cont'd)



• Select the Signal Probe ( ) tool from the tool palette.

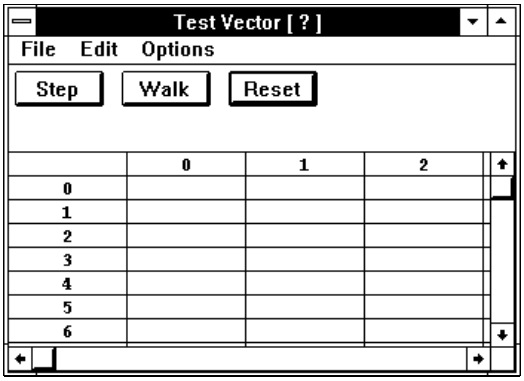
• Click and hold the probe tip on the +5V connection to the counter device, as shown. If this line indicates a "Z" value (high impedance), then it will be necessary to inject a high value.

Some earlier version of DesignWorks Schematic did not place a simulation value on signals that where connected to power or ground connectors. The power symbols in all current libraries will place the correct simulation value on the attached signal

• If the probe indicated a "Z" value above, then click and hold the probe cursor on the power signal line. While still holding the mouse button, press the "1" key. You will see the probe change to the 1 value indicating that the signal has changed state. Release the mouse button.

• Repeat this procedure on the ground line, except this time press the "0" key (if it is not already at the 0 level).

Note: This procedure only needs to be done on any one ground line, even if there are many ground symbols in the circuit. All like symbols are effectively connected together for simulation purposes.

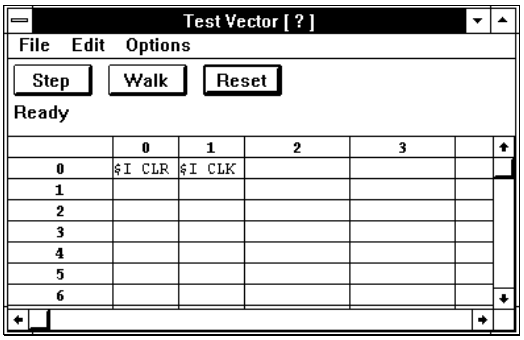


Opening a Test Vector Window

•Select Test Vector from the Tools menu in the DesignWorks window.

The Test Vector window has three main areas:

- Menus along the top.
- Execution control buttons Step, Walk and Reset.
- "Spreadsheet" data area at the bottom. You will enter your test data into this area.



Entering a Header Line

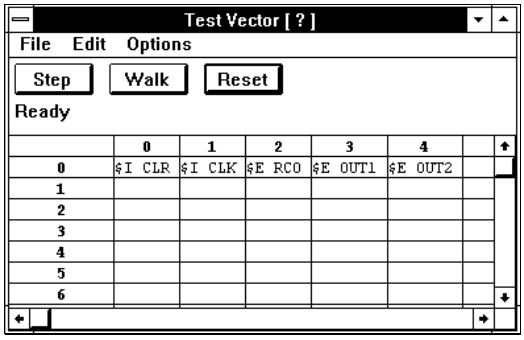
- **Double-click on the top left data cell in the spreadsheet area.**
- **Enter "$I CLR" in this cell.**

The "$" character indicates that this cell contains a command. In this case "$I" is a short form of $INPUT and indicates that this spreadsheet column is going to be used to specify input values for the signal CLR.

- **Press the Tab key to move to the next cell to the right and enter "$I CLK".**

Note: You can change the column width by clicking and dragging on a dividing line between column headers.

Entering a Header Line (cont'd)



	0	1	2	3	4
0	$I CLR	$I CLK	$E RCO	$E OUT1	$E OUT2
1					
2					
3					
4					
5					
6					

• Press the Tab key to move to the right, then enter "$E RCO".

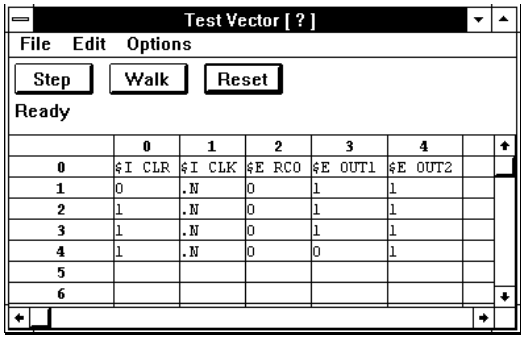
"$E" is a short form of $EXPECTED, indicating that this column will be used to specify expected values for the RCO signal. Once the simulation has settled after applying the input values on this line, the values specified in $E columns will be compared to the actual signal values.

• Enter the commands shown in the next two cells.

This top row of cells is referred to as a "header" since it specifies how the remaining cells in each column will be used. Although these commands will normally appear in the first row, you can change the definition of a column by inserting a command anywhere in the test program.

• Select the Resize Columns command from the Options menu to adjust the columns to fit.

Entering Test Vector Data



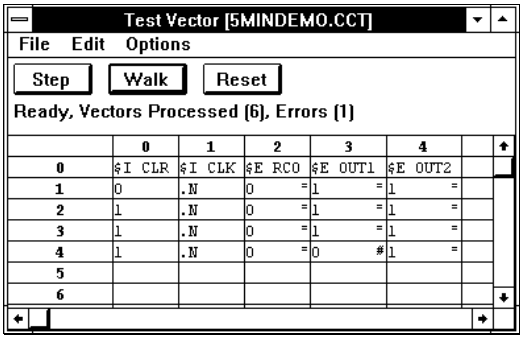
	0	1	2	3	4
0	$I CLR	$I CLK	$E RCO	$E OUT1	$E OUT2
1	0	.N	0	1	1
2	1	.N	0	1	1
3	1	.N	0	1	1
4	1	.N	0	0	1
5					
6					

• Enter the values shown in the second and subsequent rows of cells.

The value ".N" specifies a clock pulse that starts high, goes low for a period (specified in the Configuration command in the Options menu), then goes high again. This negative-going pulse is used here to allow some setup time between when the CLR input is applied and the positive clock edge.

If no value is specified in a given cell, no action is taken. I.E. in an $INPUT column, the value is left at the previous level, in an $EXPECTED column, no comparison is done.

Executing the Test Vectors



	0	1	2	3	4
0	$I CLR	$I CLK	$E RC0	$E OUT1	$E OUT2
1	0	.N	0 =	1 =	1 =
2	1	.N	0 =	1 =	1 =
3	1	.N	0 =	1 =	1 =
4	1	.N	0 =	0 #	1 =
5					
6					

• Click on the Reset button

This button ensures that the test program is ready to be executed by:

• Canceling any test vector execution currently in progress.

• Clearing any program-generated data in the spreadsheet.

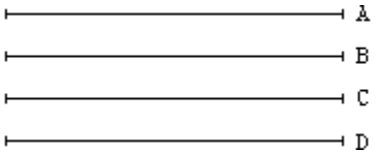
• Positioning the selection point in the top-left cell.

• Click on the Walk button.

You will now see the rows in the test program executed in sequential order. Each cell in an "expected" column that matches the evaluated value is marked with an "=" while those that don't match are marked with "#". This particular test should generate one failure.

• Close the Test Vector window and the circuit window as they will not be needed for the balance of this tutorial.

Generating a Repeating Test Pattern



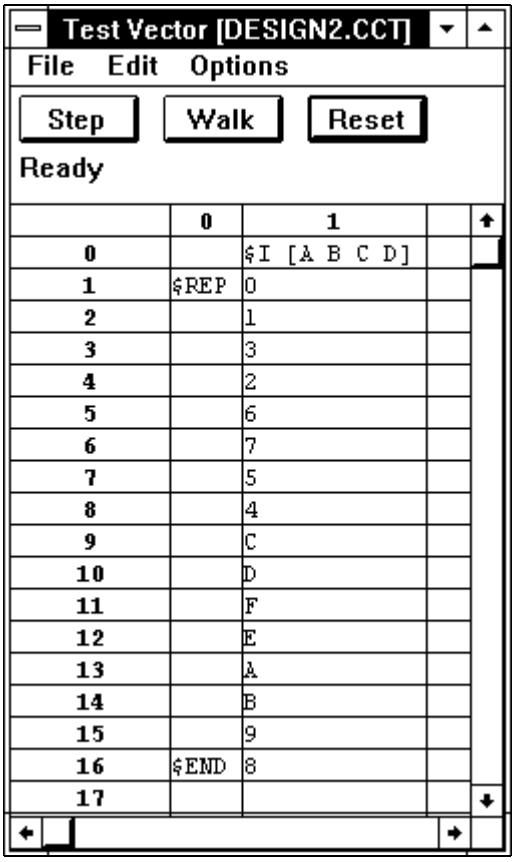
• Select the New Design command from the File menu in the DesignWorks window.

• When the Design Mode dialog appears, Select any Flat design mode.

• Click on the New Design button.

• Using the signal (+) tool, draw four parallel signal lines anywhere on the schematic.

• Using the text (T) tool, name the signals A, B, C and D, as shown.



	0	1
0		$I [A B C D]
1	$REP	0
2		1
3		3
4		2
5		6
6		7
7		5
8		4
9		C
10		D
11		F
12		E
13		A
14		B
15		9
16	$END	8
17		

Generating a Repeating Test Pattern (cont'd)

•Select Test Vector from the Tools menu in the DesignWorks window.

• Enter the text data as shown.

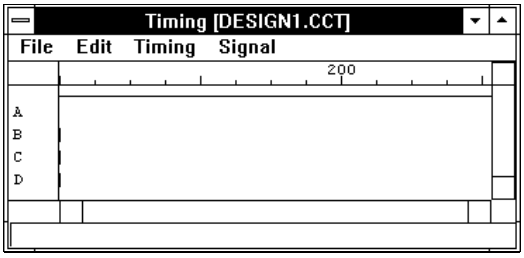
$I again indicates that this column will be used to specify signal input values. In this case we are using square brackets to provide a list of signals that will be grouped together, i.e. specified as a single hexadecimal value. The rightmost signal in the list (i.e. D in this case) will be the least significant bit of the value.

The $REP and $END commands form a repeat loop, i.e. all rows between and including the $REP and $END rows will be repeated multiple times. In this case, since no integer was given after the $REP, the loop will be executed indefinitely until stopped by the user.

• Click on the Reset and then the Walk buttons.

Execution now proceeds repeatedly through the test program.

Displaying the Test Pattern



• Select Timing from the Tools menu in the DesignWorks window.

This displays the Timing window.

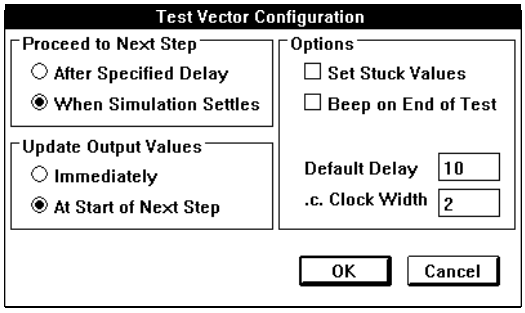
• Select signals A, B, C and D in the schematic window by clicking on them while holding the Shift key.

• Select the Add to Timing command from the Timing menu.

Note that the time value displayed in the timing window is not changing and that the waveforms are not being drawn in the timing window. The Test Vector, by default, executes the next step in the test program as soon as all simulation activity ceases from the previous step. In this case, there are no devices in the circuit to introduce a delay, so all steps are executed at the same time point.

Note:

You may see a warning dialog indicating "Not Enough Memory to Keep Simulating" and notice that the simulation time is not advancing. The simulator must keep a large amount of data in memory for screen updates. Simply click the Reset button to flush memory, restart the simulator and correct this situation.



Setting Step Size

To introduce a fixed delay regardless of circuit activity we can set a minimum delay between steps.

• Select the Configuration command from the Options menu in the Test Vector window.

• Enter the value 10 in the Default Delay box.

• Click on the "After Specified Delay" button.

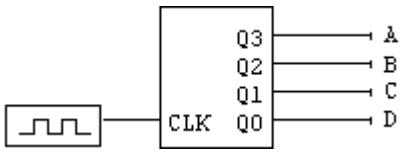
• Click on the OK button.

• Click on the Reset button then the Walk button.

You will now see that the time value will start progressing and waveforms will be drawn as expected. These waveforms will now be generated with the specified timing regardless of other simulation activity.

• Close the Test Vector window, as this test program is not needed for the balance of the tutorial.

Monitoring Circuit Activity



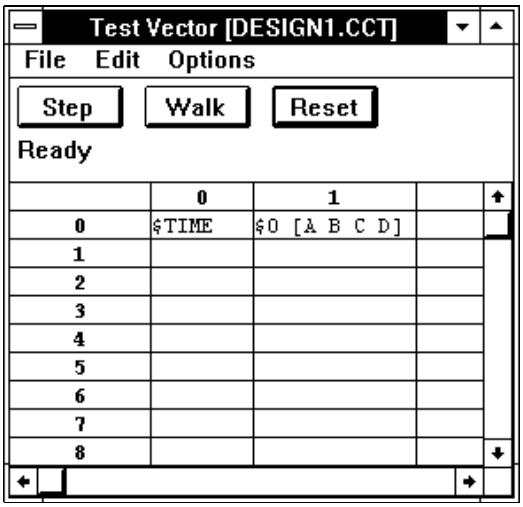
• Select a Counter-4 Min. device from the "primlog.clf" library and place it so that its outputs connect with the existing signals, as shown.

• Place a Clock device so that it drives the counter's clock input.

• Select the Clear X button in the Simulator window.

If the timing window is still open, you will see a standard count sequence appear on the displayed signals.

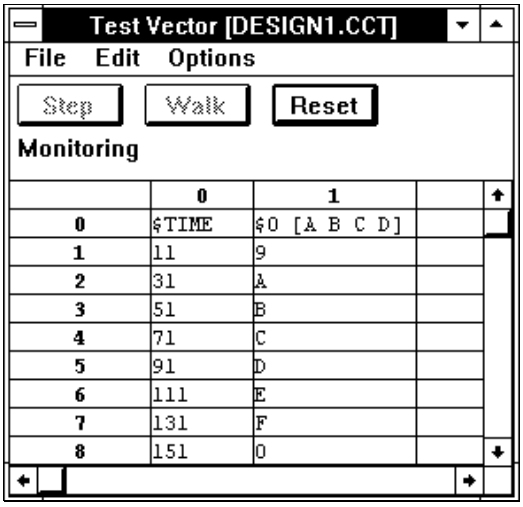
Monitoring Circuit Activity (cont'd)



- **Select Test Vector from the Tools menu in the DesignWorks window.**
- **Enter $TIME in the top left cell, and the $O [A B C D] in the next cell to the right, as shown.**

The $TIME command requests that the following cells be filled in the actual time at that step. The $O command is a short form of $OUTPUTS and requests that the Test Vector fill in the actual values of the given signals in that column. It is possible to include the same signal in all three types of columns ($I, $E and $O) to check bidirectional or multiply-driven lines.

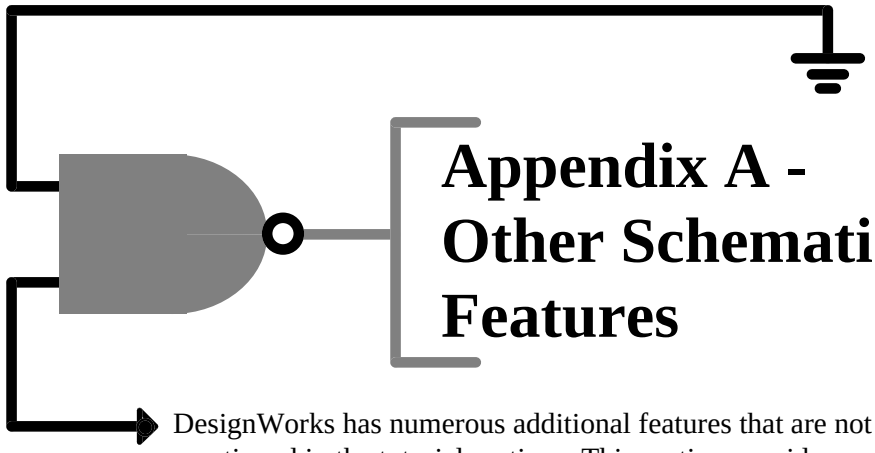
Monitoring Circuit Activity (cont'd)



- **Click on the Reset button to ensure that the top row is selected.**
- **Select the Monitor Mode command from the Options menu.**

You will notice that the cells under the $TIME and $O commands are filled in each time one of the displayed signals changes. The contents of the spreadsheet can be cleared at any time using the Reset button and can be saved to a text file using the Save Test As command from the File menu.

This completes the tutorial section “Creating and Executing Test Vectors”.



Appendix A - Other Schematic Features

DesignWorks has numerous additional features that are not directly mentioned in the tutorial sections. This section provides an overview of some of these features.

Libraries

DesignWorks™ is shipped with an extensive set of over 12,000 device symbols. Digital components are provided in Compact, ANSI (rectangular) and IEEE formats. Gate devices are provided in monolith (i.e. one package = one symbol) and with DeMorgan equivalents. All digital devices have full gate packaging information.

Family	Compact	ANSI	IEEE	Comments
Connectors	X	X		General connector symbols
Diodes	X			Various standard diode types
Discretes	X			Common discrete components
National Linear	X	X		Linear ICs
Transistors	X			Various standard transistor types
Spice Lib	X			For SPICE-based simulators
Primitives	X			DesignWorks simulation primitives
54 TTL	X	X	X	Includes 54, 54S, 54LS, 54AS, 54ALS, 54AC, 54ACT, 54F, 54HC, 54HCT, 54HCU
74 TTL	X	X	X	Includes 74, 74S, 74LS, 74AS, 74ALS, 74AC, 74ACT, 74F, 74HC, 74HCT, 74HCU
75 TTL	X	X	X	Includes 75ALS
CMOS	X	X	X	GE/RCA CMOS
ECL	X	X	X	National ECL
Memory	X	X	X	Motorola, Texas Instruments (TI) and Toshiba
MicroProcessors	X	X	X	Intel, Motorola and Zilog
Miscellaneous	X	X	X	
PLD	X	X	X	Note: When used with MacABEL, PLD symbols are auto-generated from the MacABEL library.

Find and ErrorFind Tools

The Find tool allows you to interactively locate devices, pins or signals by name or attribute value. Matching items can be viewed one at a time, or all items can be selected at once and then accessed with another tool.

The ErrorFind tool is similar to Find, but locates items by possible error conditions, including:

- Unnamed devices
- Unnamed signal
- Multiply driven signal
- Fanout > X
- Unconnected pin
- Unmatched port pin
- Unmatched port connector
- Undriven signal
- Unconnected signal
- Unmatched page connector
- Unnumbered pin

Any located errors can be flagged as OK so they are not located again.

Report Generation

DesignWorks includes a powerful Custom Report Generator tool for netlist and text report generation. The report format is driven by a "form file" which contains formatting commands and constant text. Form file features allow you to control:

- Overall report structure, e.g. netlist formats by signal or by device, listings by device for bills of materials, etc.
- Design, device, signal and pin attributes to be included.
- Selection of devices or signals to include in the report, by name or attribute value.
- Selection of attribute fields to be used as sources for power and ground connections.
- Sorting and merging of lines within the file.
- Format of each pin connection entry, each line and each page.
- Hierarchy format, including flattened and hierarchical netlists.
- Error checking, including checking for missing attribute fields.

The package includes 20 or more form files for standard industry formats. These can be used as-is or used as a guide for creating your own formats.

Custom Sheet Settings

DesignWorks supports full customization of sheet borders, grids and graphics. The default border which is created for each new design can be updated from a "sheet template" file with a single operation. Template files are really just design files with custom settings for border size, text font, grid spacing, company logo, etc. Templates for the standard ANSI sizes A - E and other common sizes are included.

Appendix A - Other Schematic Features

Attribute Operations

DesignWorks™ allows text attributes to be associated with any device, signal or pin in a design, and with the design itself.

Attribute Editing - Attributes can be entered individually on each object through a standard select and Get Info operation. Any attribute that is displayed on the schematic can be edited right on the schematic.

Attribute Display Options - Attributes can be displayed on the schematic adjacent to the associated signal, device or pin. Each field can be moved and rotated individually. A default display position can be specified for device attributes. Field names can be optionally displayed with each item. Text style for attribute display is set globally for all attributes in the design.

Attribute Global Operations - Attributes are defined centrally for a design. Global Duplicate, Merge and Delete operations allow all data associated with a field to be modified throughout the design. User-defined attribute fields can be added at any time.

Report Generation - All attribute fields can be used in custom report formats.

Hierarchy and Part Type Operations

DesignWorks™ provides a number of powerful operations for working with device or hierarchical block symbols and internal circuit definitions.

Hierarchy Mode - Three hierarchy modes are available to accommodate different design requirements. "Flat" mode provides the simplest possible structure for smaller designs. "Pure" mode implements a pure hierarchical structure, i.e. each part type is defined only once and all instances of a type are identical. "Physical" mode allows full hierarchical operation, but allows separate attribute data to be associated with each physical instance of a part.

Hierarchy Operations - Hierarchical designs can be created "top-down" or "bottom-up". Attach and Detach commands allow separately-created designs to be merged into a single hierarchy, or vice-versa. Internal circuit definitions can be saved to a separate circuit file. Part definitions can be saved from a schematic sheet to a library. Devices in a schematic can be updated from their original library or from any selected new source.

Back Annotation

The DesignWorks Back Annotation allows device package assignments to be automatically updated from a "was-is" text file created by an external system. Formats supported include Pads, Cadnetix (SCICARDS), Douglas, Racal-Redac RINF and XCAD. Pin swaps, gate swaps and component renaming are supported in flat or hierarchical designs.

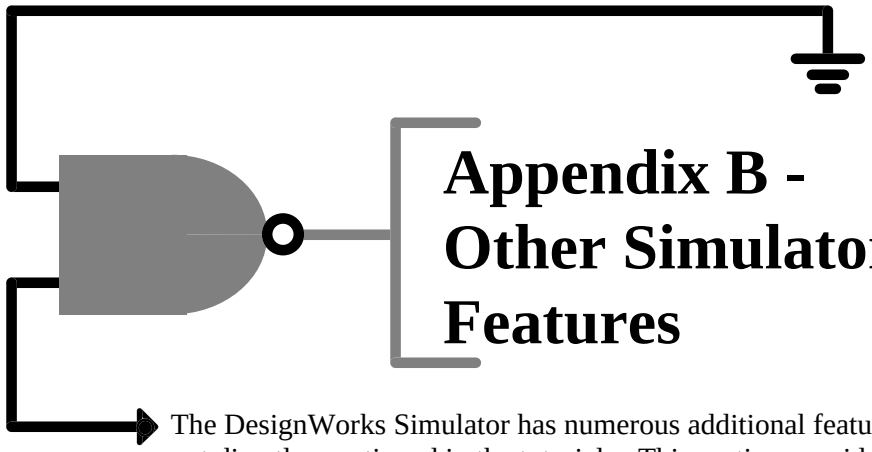
Optional EDIF (Electronics Data Interchange Format) Schematic Translator

An optional translator for the standard EDIF 2 0 0 data format is available for DesignWorks. This data format allows schematics, netlists and parts libraries to be exchanged between design systems produced by different manufacturers. The EDIF format can be read and written by most workstation-based ECAD systems and a growing number of personal computer-based packages.

Optional FPGA Design Kits

A number of optional design kits are available for using DesignWorks to generate and simulate designs for Field Programmable Gate Arrays. These design kits include symbol libraries matching the chip manufacturer's databook, a netlist generator and, in some cases, back annotation of post-layout delays.

An example of a design for the Xilinx 3000 series is included on the demonstration disk.



Appendix B - Other Simulator Features

The DesignWorks Simulator has numerous additional features that are not directly mentioned in the tutorials. This section provides an overview of some of these features.

Simulation Attribute Operations

The simulation tools make extensive use of DesignWorks text attributes:

- Sets of test vectors can be saved to and loaded from design attributes.
- Delay values for any group of devices or pins can be saved to or loaded from device or pin attributes. This allows loading and testing of Min/Max/Typ delays for any group of objects.
- Initial values for signals and pins can be specified in attributes.
- An optional "input value map" can be specified in a design attribute field. This allows the user to specify the treatment of high impedance and "don't know" input values for the entire design.
- Design attribute fields are used to save setups for the timing tool and trigger facilities.

Simulation Text File Operations

The Timing and Test Vector tools use a common data format for saving and loading timing data. This format is in a simple tab-delimited format that can be read by most spreadsheet and database packages for external interpretation.

The Test Vector tool also has a "trace file" option that writes a line to a disk file each time a test vector is executed. This allows a continuous record of simulation results to be kept without consuming main memory.

Simulation in Hierarchical Designs

The DesignWorks Simulator is fully interactive across a hierarchical design with any number of nesting levels. The following features are available for simulation in hierarchical designs:

- Simulation can be used in "Flat" or "Physical" hierarchy modes. Simulation is not supported in "Pure" hierarchy mode.
- Internal circuit blocks can be opened and closed at will while the simulation is running for editing and probing.
- Signals in any open circuit can be displayed in the timing window or test vector window. Signal names can optionally be displayed in the timing window in hierarchical format, i.e. prefixed by the names of parent blocks.
- A Scope command allows simulation to be restricted to specific sub-circuits. This allows parts of a design to be isolated for experimentation or verification without interference from other blocks.
- Pin delays can be specified independently for each instance of a hierarchical block. This allows signal path delays to be customized based on actual layout information without modifying the definition of a block.

Optional Microprocessor Libraries

An optional set of simulation models for microprocessor devices is available for use with the DesignWorks Simulator. These models provide full bus functionality, including read, write, interrupt and error cycles. The models do not execute instructions. Models are included for 6809, 6809E, 68000, 68020, 68030, 68HC11, 8031, 8051, 8751, 8086, 8088.

Appendix B - Other Simulation Features

Model Libraries

DesignWorks Simulator is shipped with an extensive set of models for 74XX and 4000-series CMOS devices. The following table lists the models currently supported. New models are added periodically.

74XX00	74XX11160	74XX11821	74XX150	74XX198	74XX283
74XX01	74XX11161	74XX11822	74XX151	74XX199	74XX284
74XX02	74XX11162	74XX11823	74XX152	74XX20	74XX285
74XX03	74XX11163	74XX11824	74XX153	74XX21	74XX286
74XX04	74XX11168	74XX11825	74XX154	74XX2140	74XX290
74XX05	74XX11169	74XX11826	74XX155	74XX22	74XX293
74XX06	74XX11174	74XX11827	74XX156	74XX221	74XX295
74XX07	74XX11175	74XX11828	74XX157	74XX224	74XX298
74XX08	74XX11181	74XX11841	74XX158	74XX2240	74XX29806
74XX09	74XX11190	74XX11842	74XX159	74XX2242	74XX29809
74XX10	74XX11191	74XX11843	74XX16	74XX23	74XX29821
74XX1000	74XX11192	74XX11844	74XX160	74XX230	74XX29822
74XX1002	74XX11193	74XX11845	74XX161	74XX231	74XX29823
74XX1003	74XX11194	74XX11846	74XX162	74XX237	74XX29824
74XX1004	74XX112	74XX11861	74XX163	74XX238	74XX29825
74XX1005	74XX11238	74XX11862	74XX164	74XX239	74XX29826
74XX1008	74XX11239	74XX11863	74XX1640	74XX24	74XX29827
74XX1010	74XX11240	74XX11864	74XX1645	74XX240	74XX29828
74XX1011	74XX11241	74XX11873	74XX165	74XX241	74XX29841
74XX1020	74XX11244	74XX11874	74XX166	74XX242	74XX29842
74XX1032	74XX11245	74XX11881	74XX167	74XX243	74XX29843
74XX1034	74XX11251	74XX11882	74XX168	74XX244	74XX29844
74XX1035	74XX11253	74XX12	74XX169	74XX245	74XX29845
74XX1036	74XX11257	74XX120	74XX17	74XX246	74XX29846
74XX107	74XX11258	74XX121	74XX170	74XX247	74XX29861
74XX109	74XX11280	74XX122	74XX171	74XX248	74XX29862
74XX11	74XX11286	74XX123	74XX172	74XX25	74XX29863
74XX110	74XX11299	74XX1240	74XX173	74XX250	74XX29864
74XX11000	74XX113	74XX1242	74XX174	74XX251	74XX299
74XX11002	74XX11323	74XX1244	74XX175	74XX253	74XX30
74XX11004	74XX11352	74XX1245	74XX176	74XX2540	74XX31
74XX11008	74XX11353	74XX125	74XX177	74XX2541	74XX32
74XX11010	74XX11373	74XX126	74XX178	74XX257	74XX322
74XX11011	74XX11374	74XX128	74XX180	74XX258	74XX323
74XX11013	74XX11378	74XX13	74XX1804	74XX259	74XX33
74XX11014	74XX11379	74XX130	74XX1804	74XX26	74XX34
74XX11020	74XX114	74XX131	74XX1805	74XX260	74XX348
74XX11021	74XX11520	74XX132	74XX1805	74XX261	74XX35
74XX11027	74XX11521	74XX132	74XX1808	74XX2620	74XX350
74XX11030	74XX11533	74XX133	74XX1808	74XX2623	74XX352
74XX11032	74XX11534	74XX134	74XX181	74XX264	74XX353
74XX11034	74XX11568	74XX135	74XX182	74XX2640	74XX354
74XX11074	74XX11569	74XX136	74XX183	74XX2645	74XX355
74XX111	74XX116	74XX137	74XX1832	74XX265	74XX356
74XX11109	74XX11620	74XX138	74XX19	74XX266	74XX36
74XX11112	74XX11623	74XX139	74XX190	74XX27	74XX365
74XX11132	74XX11640	74XX14	74XX191	74XX273	74XX366
74XX11138	74XX11643	74XX140	74XX192	74XX276	74XX367
74XX11139	74XX11646	74XX143	74XX193	74XX278	74XX368
74XX11151	74XX11648	74XX145	74XX194	74XX279	74XX37
74XX11153	74XX11651	74XX147	74XX195	74XX28	74XX373
74XX11157	74XX11652	74XX148	74XX196	74XX280	74XX374
74XX11158	74XX1181	74XX15	74XX197	74XX282	74XX375

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74XX4514
74XX4515
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74XX53
74XX533
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