

Name: _____ Student No. _____

CSE370 Final Exam (Dec 14, 1999)

There are 4 problems for a total of 100 points. The point value of each problem is indicated in the table below. I will try to stick to the point values this time!

Each problem is on a separate sheet of paper. Write your answer neatly in the space provided. If you need more space (you shouldn't), there are a couple of extra sheets at the end of the exam, but please make sure that you indicate clearly the problem to which the comments apply.

Please do not ask or provide anything to anyone else in the class during the exam. Make sure to ask clarification questions early so that both you and the others may benefit as much as possible from the answers.

Problem 1 (18): _____

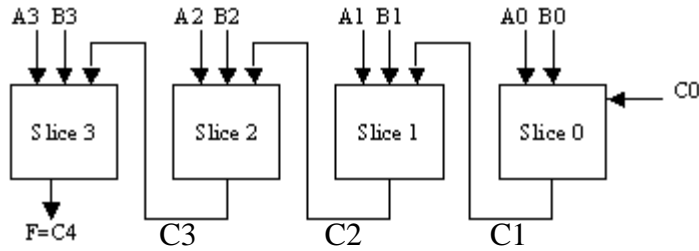
Problem 2 (24): _____

Problem 3 (28): _____

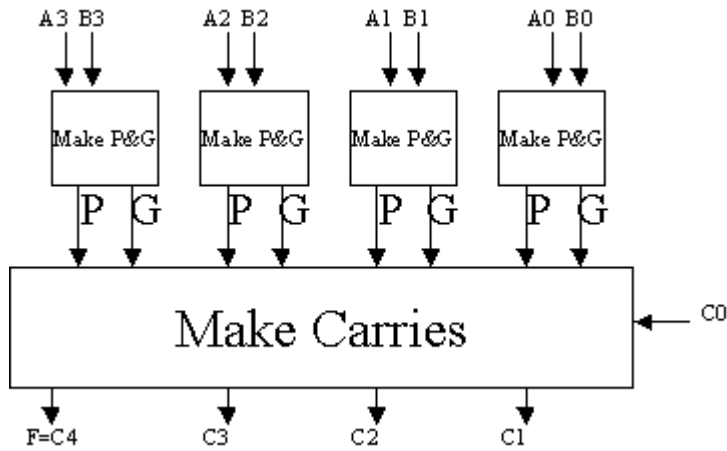
Problem 4 (30): _____

Problem 1: Carry Lookahead.

A four-bit ripple carry comparator ($F = A > B$) is shown below. In general, $C_{i+1} = 1$ if $\{A_i..A_0\} > \{B_i..B_0\}$. For example, C_2 is true if $(A_1A_0 > B_1B_0)$, so $F = C_4$.



A carry lookahead design of the same function is shown below.



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Part A: Make P&G (9)

Determine the Boolean logic equations for P_i and G_i given A_i and B_i .

- $G_i = 1$ if and only if A_i and B_i generate a carry
- $P_i = 1$ if and only if A_i and B_i propagate a carry, but do not generate one.

Find POS expressions for $P_i(A_i, B_i)$ and $G_i(A_i, B_i)$, show your work.

$P_i =$ _____

$G_i =$ _____

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Part B. Make Carries. (9)

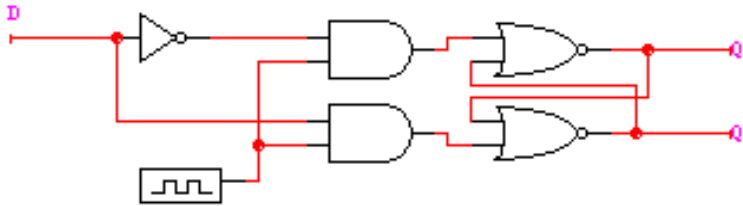
Write a two level equation for $C_4(C_0, P_3..P_0, G_3..G_0)$. It might help for you to write the equations for C_1, C_2 , and C_3 first to get the idea.

$C_4 =$ _____

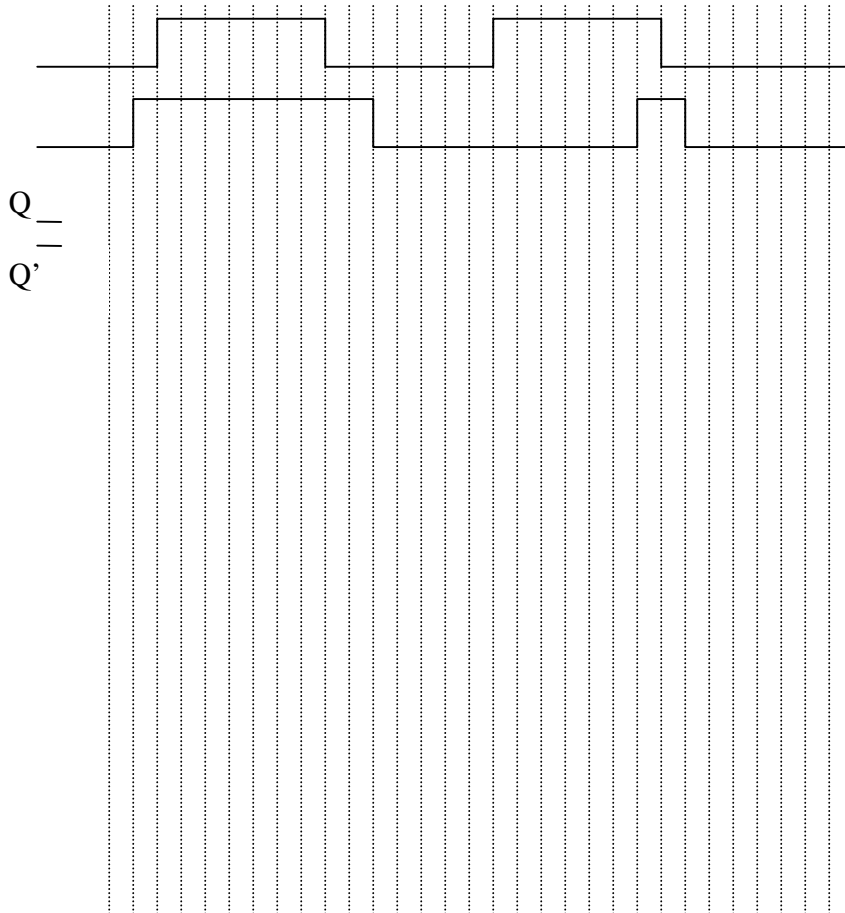
If all gates count as 1 delay (except input inversions), what is the worst delay from any input to C_4 . Explain.

Problem 2: Storage Elements

Consider the storage element shown below.



Part A (12). Assuming all gates have a 10ns delay (including the inverter) complete the timing diagram below, each time division is 10ns. Feel free to add additional signals to the timing diagram if it will help you think it through.



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Part B (12pts). What are the setup, hold, and propagation delays for this storage element (see definitions below). In each case, be specific about the edge of the clock from which you are measuring time. Explain your answers.

- T_{prop} is defined as the CLK to Q delay, assuming that D is stable.
- T_{su} is defined as the minimum time before the latching clock edge during which D must remain stable to ensure proper operation of the latch
- T_{h} is defined as the minimum time after the latching clock edge during which D must remain stable to ensure proper operation of the latch.

3. State Machine Design

Design a 2-bit synchronous “skip counter” that has two control inputs: C (for “count”) and S (for “skip”). If C is asserted then the value in the counter will be incremented by 1. If C is not asserted and S is asserted then the value in the counter will be incremented by 2, otherwise the value in the counter remains unchanged. The system has two outputs V1 and V0 that indicate the current value of the count. The following table fully specifies the function of the skip-counter:

C	S	Cur. State	Next State	V1,V0
0	0	n	n	n
0	1	n	n+2	n
1	-	n	n+1	n

Where $0 \leq n \leq 3$

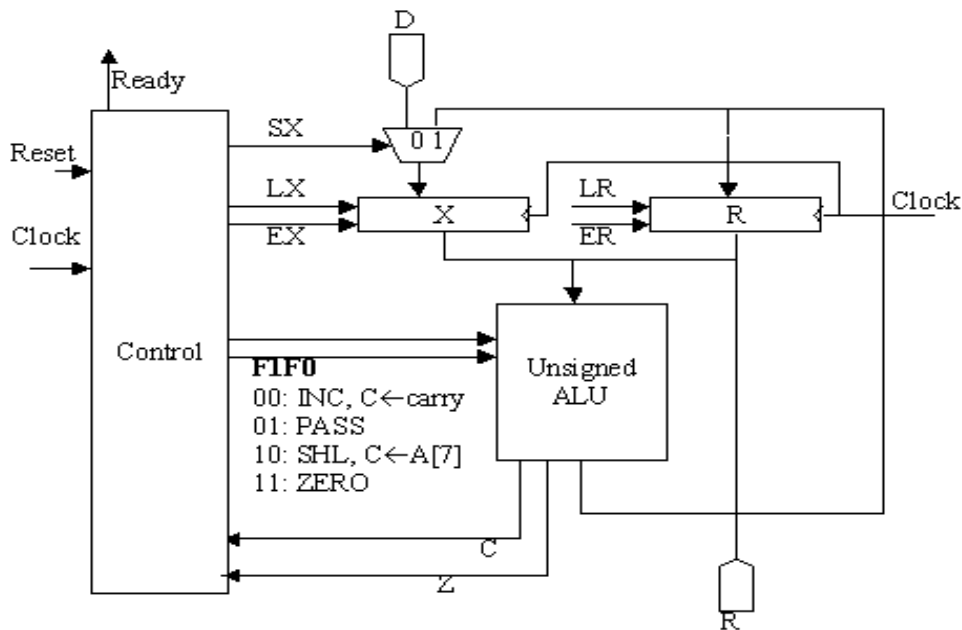
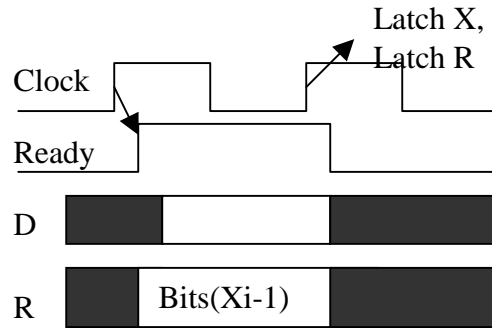
Part A (14). Draw the complete finite state machine diagram.

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Part B (14). Using *output encoding*, and positive edge triggered D flip-flops, determine the minimized two-level next state functions and draw the complete state machine schematic clearly indicating inputs and outputs. Assuming 1 time unit per gate, $T_{su} = 4$, and $T_p = 2$, what is the minimum clock period for your counter?

Problem 4. Controller Design

Given the following 8-bit datapath and associated control points, the problem is to design a controller to count the number of 1's in the input data byte (D). The timing interface shown is the same as it was for the multiplier, except that there is only one data value to read. [When you assert Ready, the input data (X_i) value will be available on D until the end of that clock cycle, and you must ensure that the result of the previous computation, $R = \text{Bits}(X_{i-1})$, is available until the end of the that clock cycle.]



Inputs and Control Points:

- SX: Select D or ALU output to load into X (if LX is asserted)
- LX: Load X (1 is load, 0 is hold)
- EX: Enable X output (1 is enabled, 0 is tri-stated)
- ER: Enable R output (1 is enabled, 0 is tri-stated)
- LR: Load R (1 is load, 0 is hold)
- F1,F0: Opcode for ALU as defined above. ZERO sets the output to zero regardless of the inputs.
- D: Data input

Outputs

- Z: Zero condition code. Set any time the result of an ALU operation is zero
- C: Carry condition code. Set by SHL ($C \leftarrow A[7]$), and INC.
- R: Data output.

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Part A (15). Design the controller state diagram. For each state, indicate the register transfer operation that is being performed and indicate which control lines are asserted in that state. You can use as many states as you like, but you shouldn't need more than FOUR. Be sure to identify your reset state.

Part B. Do one of the following two options. You do NOT need to come up with minimized expressions for your logic. Make sure to include the synchronous Reset input in your design.

Option 1 (15): If you can, implement your state machine using the 2-bit skip counter from Problem 4, slightly modified below, as your only storage element. The skip counter definition has been modified by the addition of an asynchronous reset input (R) as defined in the table below.

Modified 2-bit Skip Counter (R input added)

R	C	S	Cur. State	Next State	Count (V1,V0)
0	0	0	n	n	n
0	0	1	n	n+2	n
0	1	-	n	n+1	n
1	-	-	n	0	n

Where $0 \leq n \leq 3$

Option 2 (10): Otherwise use a regular counter with R,L,C control inputs that work according to the following function table. Your regular counter can have as many bits as you need.

Regular m-bit counter (R input added)

R	L	C	D	Cur. State	Next State	Count (Vm...V0)
0	0	0	-	n	n	n
0	0	1	-	n	n+1	n
0	1	-	m	n	m	n
1	-	-	-	n	0	n

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