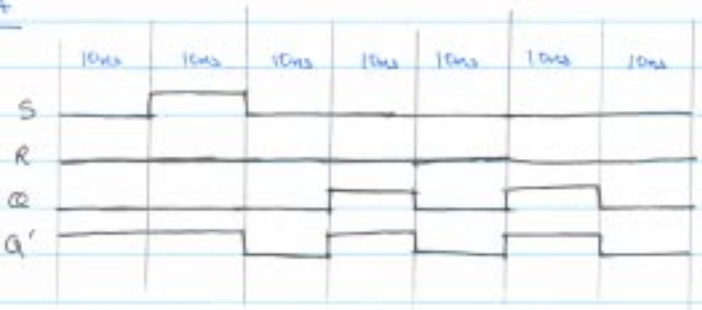
CSE 370 Fall '99
Solution 7.

PART A



So as seen above the latch keeps on toggling. The reason for this behaviour is that the effect of setting the latch takes TWO gate delay. to propogate from S → Q. So Q' must remain LOW for that time.

=>

Minimum Pulse required is 20ns.

PART B

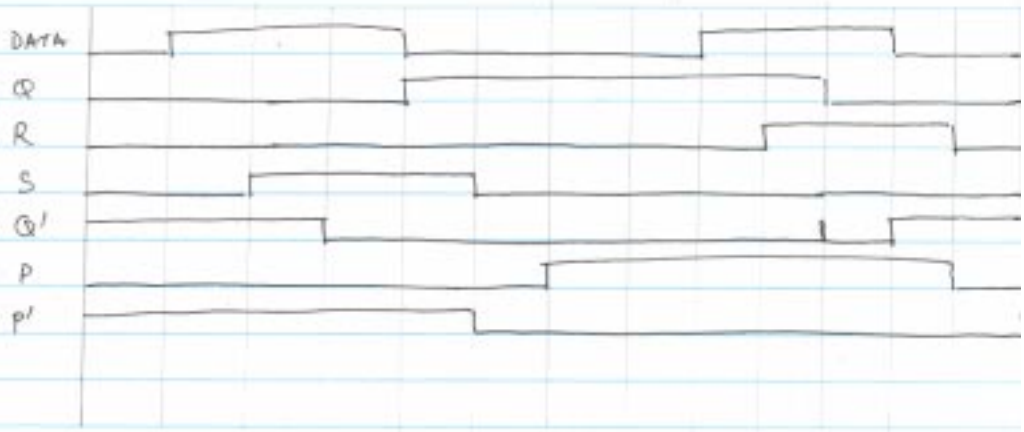
$$Q^{\uparrow} = (R+Q')'$$
$$Q'^{\uparrow} = (S+Q)'$$
$$S^{\uparrow} = (Q' \cdot DATA)$$
$$R^{\uparrow} = (Q \cdot DATA)$$

As seen above there is a potential for a glitch in R and S, which can also propogate. Note that there is still exactly one state transition per input pulse so the circuit IS CORRECT.

Adding a further 20ns delay between P and Q (and b/w P' and Q') gets rid of this glitch

There are various ways of adding this delay like.

etc.



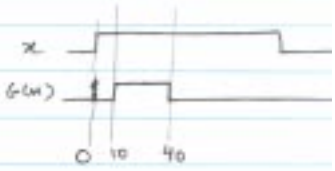
$$Q^{+} = (R + Q')'$$
$$Q'^{+} = (S + Q)'$$
$$S^{+} = (P' \cdot DATA)$$
$$R^{+} = (P \cdot DATA)$$
$$P^{++} = Q$$
$$P'^{++} = Q'$$

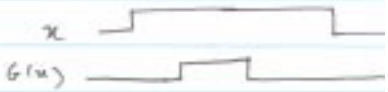
As seen above there is no glitch (or possibility of it). as no two inputs to the SAME gate change at the same time.

PART C

Width of the pulse = $0.1\overline{36}$ seconds.

To generate a glitch of 30ns, following circuits would do it
(Assuming each gate as 10ns delay)





PART D

Sensor 1	Sensor 2	Q(t)=P(t)	Q(t+1)	R	S
0	0	0	0	X	0
0	0	1	1	0	X
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	X	X	X
1	1	1	X	X	X

Minimizing this one gets.

$R(P, S1, S2) = P(S1 + S2)$

$S(P, S1, S2) = P'(S1 + S2)$

So combining everything, the whole circuit looks like.