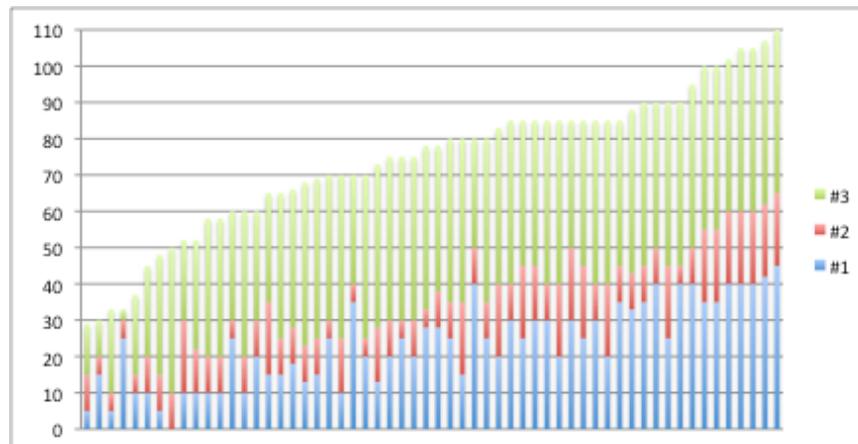


Exam 2 Results

- Average = 74; Median = 78; StDev = 20 (68% within 54 and 94)
 - Q1 avg = 23.4/45; Q2 avg = 12.3/20; Q3 avg = 38.4/45



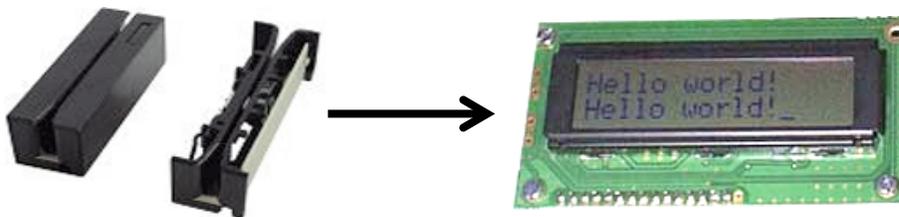
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CSE370 - XI - Programmable Logic

1

Final Lab Project

- Magnetic stripe card reader to LCD display
- Given:
 - basic schematic
 - test fixtures
- Your job:
 - design the core of the system



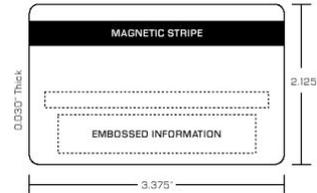
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CSE370 - XVIII - Final Lab Project

2

Overview of Magnetic Stripe Cards

- Commonly used in credit, debit, transportation, and gift cards
- Magnetic material (iron-ion rich) is contained in a plastic-like film
 - Stripe is 5.66 mm from edge of card and is 9.52 mm wide
 - Contains three tracks, each 2.79 mm wide
 - Tracks one and three are typically recorded at 8.27 bits per mm
 - Track two typically has a recording density of 2.95 bits per mm
- Various ISO standards define format
 - 7810, 7811, 7812, 7813, and 4909
 - Defined by each industry



See http://en.wikipedia.org/wiki/Magnetic_stripe_card for details

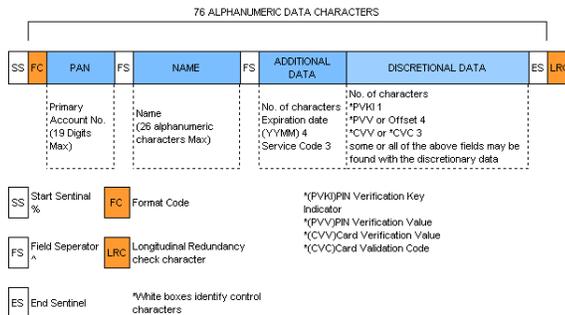
0.223"	TRACK	Recording Density (Bits per inch)	Character Configuration (including parity bit)	Information Content (including control characters)
0.110"	1 IATA	210	7 bits per character	79 alphanumeric characters
0.110"	2 ABA	210	5 bits per character	40 numeric characters
0.110"	3 THRIFT	210	5 bits per character	107 numeric characters

Overview of Magnetic Stripe Cards

- Data encoded as 7-bit characters
 - 6 bits for value (least significant bit first)
 - 1 bit for parity

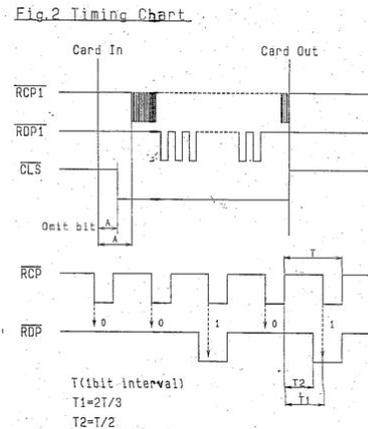
BIT				CHARACTER SET			
b ₄	b ₃	b ₂	b ₁	b ₅	0	1	1
0	0	0	0	0	SP	8	P
0	0	0	1	1	!	1	Q
0	0	1	0	0	*	2	R
0	0	1	1	1	#	3	S
0	1	0	0	0	\$	4	T
0	1	0	1	0	%	5	U
0	1	1	0	0	&	6	V
0	1	1	1	1	'	7	W
1	0	0	0	0	(8	X
1	0	0	1	1)	9	Y
1	0	1	0	0	+	:	Z
1	0	1	1	1	,	[
1	1	0	0	0	<	\	
1	1	0	1	0	=]	
1	1	1	0	0	>	^	
1	1	1	1	1	/	_	

Card Data Format - Track 1



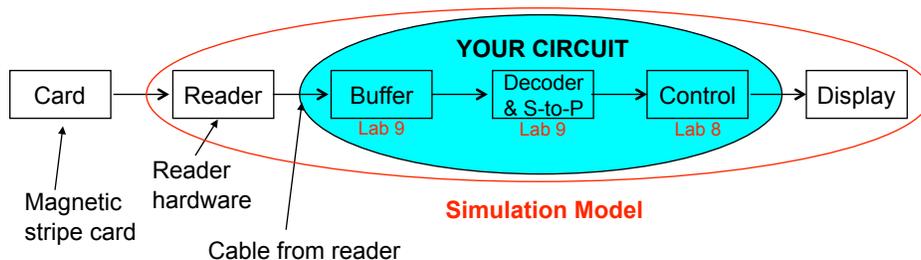
Reader serial data format

- 3 signals
 - RCP – “clock”
 - RCP only oscillates if card is moving
 - RDP – data
 - CLS – card “present” indicator
 - CLS is only active if a card is present
- Decoding
 - Use RCP falling transition to sample RDP when CLS is asserted



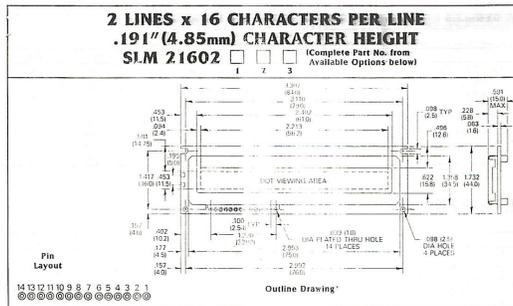
Block diagram

- Major components
 - Reader outputs (simulation test fixture)
 - **LCD controller (Lab 8)**
 - **Reader buffer, decoder, and serial-to-parallel converter (Lab 9)**
 - LCD display (simulation test fixture)



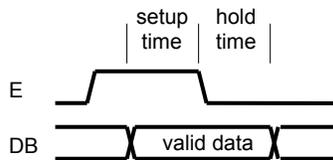
LCD interface

- Eleven signal wires plus PWR/GND/V₀
 - 1 mode input
 - 1 read/write control
 - 1 enable
 - 8 data lines (bi-directional)



Interface Pin Connections

Pin No.	Symbol	Function
1	V _{SS}	0V
2	V _{DD}	-5V
3	V ₀	—
4	RS	H: Data input L: Instruction input
5	R.W	H: Read(MPU ← LCM) L: Write(MPU → LCM)
6	E	Enable signal
7	DB0	Data bus line
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	

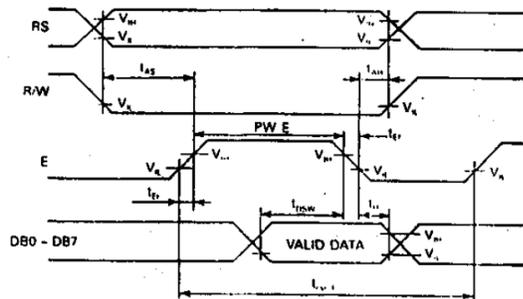


Basic LCD operations

- Requires sequence of 4 instructions/commands on initialization (**RS = 0**)
 - **Command write (RW = 0)** – data bus pins carry command code
- Many more instructions/commands (**RS = 0**)
 - E.g., backup cursor, blink, etc. (look up appropriate DB values)
- Printing a character to the display (**RS = 1**)
 - **Data write (RW = 0)** – data bus pins carry character to display
- Read busy signal (on DB7)
 - LCD uses it to force a wait
 - **RW = 1**
 - Need to make sure not driving data lines (DB = 8'bzzzzzzzz)
 - Use DB7 as input, check if 0 (not busy) or 1 (busy)

Operation	RS	DB7...DB0
Clear Display	0	0000 0001
Function Set	0	0011 0011
Display On	0	0000 1100
Entry Mode Set	0	0000 0110
Write Character	1	DDDD DDDD

Timing details



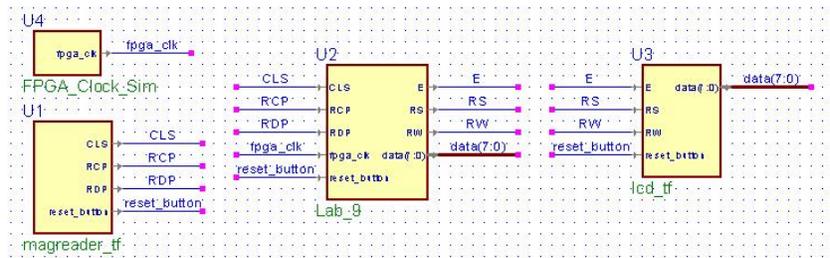
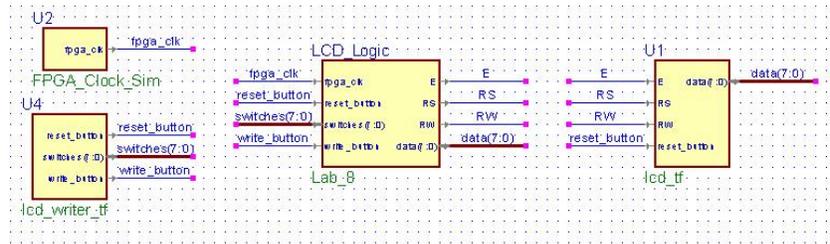
WRITE OPERATION					
Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{CYC,E}$	1.0	—	—	μ s
Enable Pulse Width	PW E	450	—	—	ns
Enable Rise/Fall Time	t_{E}, t_{E}	—	—	25	ns
Address Set-up Time	t_{AS}	140	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Data Start-up Time	t_{D}	195	—	—	ns
Data Hold Time	t_{DQ}	10	—	—	ns

ASCII codes

CHARACTER FONT DATA CODES

		UPPER 4-BIT HEXADECIMAL															
		0	1	2	3	4	5	6	7	A	B	C	D	E	F		
Higher 4-bit	Lower 4-bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111			
0	xxxx0000	00P	0P														
1	xxxx0001	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa	!@Qa		
2	xxxx0010	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B	"2B		
3	xxxx0011	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C	#3C		
4	xxxx0100	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D	\$4D		
5	xxxx0101	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E	%5E		
6	xxxx0110	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F	&6F		
7	xxxx0111	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G	'7G		
8	xxxx1000	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H	(8H		
9	xxxx1001)9I)9I)9I)9I)9I)9I)9I)9I)9I)9I)9I)9I)9I)9I		
A	xxxx1010	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J	*:J		
B	xxxx1011	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K	+;K		
C	xxxx1100	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L	,<L		
D	xxxx1101	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M	-=M		
E	xxxx1110	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N	.>N		
F	xxxx1111	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O	/?O		

Block Diagrams for Labs 8 and 9



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CSE370 - XVIII - Final Lab Project

11

Purpose of the project

- Learn how to build a complete system that does something useful
- Read data sheets
- Use communicating state machines
- Use test fixtures and read some more complex Verilog code

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CSE370 - XVIII - Final Lab Project

12