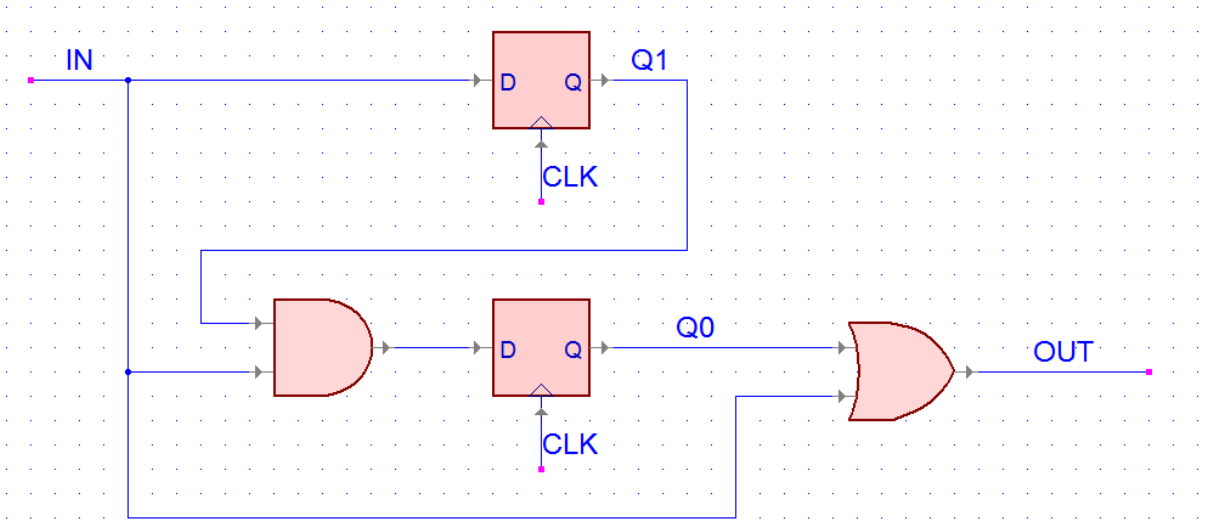
Name_____

CSE 370 – Introduction to Digital Logic Design
Spring 2010
Quiz #6

For maximum credit, show all your work. Please raise your hand if you have a question.



Complete the timing diagram that shows the execution of the circuit above. Assume that the gates and registers have a delay of 1ns. The vertical dotted lines break the time line into 1ns sections. (Thus the clock period is 8ns.) You do not have to think about setup and hold times.