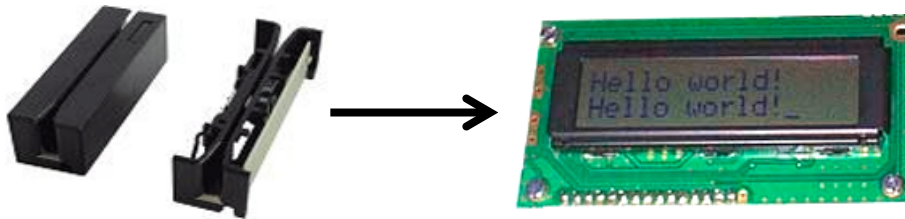


Final Lab Project

- Magnetic stripe card reader to LCD display
- Given:
 - basic schematic
 - test fixtures
- Your job:
 - design the core of the system



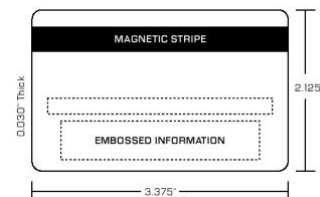
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1

Overview of Magnetic Stripe Cards

- Commonly used in credit, debit, transportation, and gift cards
- Magnetic material (iron-ion rich) is contained in a plastic-like film
 - Stripe is 5.66 mm from edge of card and is 9.52 mm wide
 - Contains three tracks, each 2.79 mm wide
 - Tracks one and three are typically recorded at 8.27 bits per mm
 - Track two typically has a recording density of 2.95 bits per mm
- Various ISO standards define format
 - 7810, 7811, 7812, 7813, and 4909
 - Defined by each industry



See http://en.wikipedia.org/wiki/Magnetic_stripe_card for details

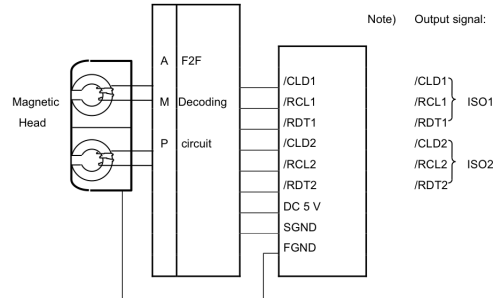
0.223"	TRACK	Recording Density (Bits per inch)	Character Configuration (including parity bit)	Information Content (including control characters)
0.110"	1 IATA	210	7 bits per character	79 alphanumeric characters
0.110"	2 ABA	210	5 bits per character	40 numeric characters
0.110"	3 THRIFT	210	5 bits per character	107 numeric characters

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2

Magnetic Card Interface



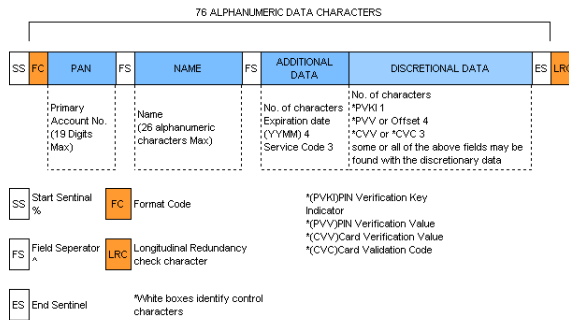
- (1) /CLD(CARD LOAD) : The /CLD line will be Low when a Magnetic Card is running in the Magnetic Card Reader. The /CLD line will be High when the Card is stopped or not present in the Card reader.
- (2) /RCL(READ CLOCK) : This is used to sample the data line by it's falling edges. The time relationship of the clock with respect to the order signals is shown in Figure 6.4.
- (3) /RDT(READ DATA) : The moment /RCL change from High to Low ; /RDT is "1" when the /RDT line is Low , and /RDT is "0" when the /RDT line is High.

Overview of Magnetic Stripe Cards

- Data encoded as 7-bit characters
 - 6 bits for value (least significant bit first)
 - 1 bit for parity

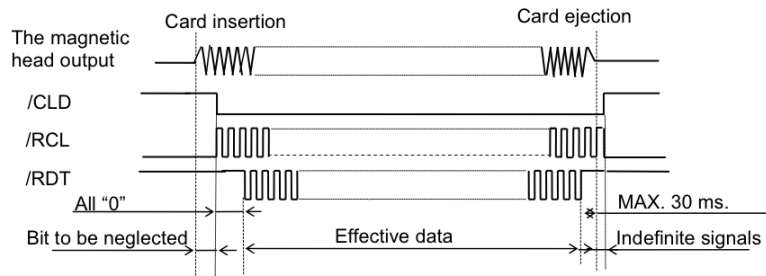
BIT				CHARACTER SET			
b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	0	1
0	0	0	0	0	0	SP	␣
0	0	0	1	0	0	!	A
0	0	1	0	0	0	*	B
0	0	1	1	0	0	#	C
0	1	0	0	0	0	\$	D
0	1	0	1	0	0	%	E
0	1	1	0	0	0	&	F
0	1	1	1	0	0	'	G
1	0	0	0	0	0	(H
1	0	0	1	0	0)	I
1	0	1	0	0	0	+	J
1	0	1	1	0	0	,	K
1	1	0	0	0	0	.	L
1	1	0	1	0	0	-	M
1	1	1	0	0	0	>	N
1	1	1	1	0	0	/	O

Card Data Format - Track 1



Reader serial data format

- 3 signals
 - /RCP(RCL) – “clock”
 - RCP only oscillates if card is moving
 - /RDP(RDT) – data
 - CLS is only active if a card is present
- Decoding
 - Use RCP falling transition to sample RDP only when CLS is asserted



Clock and Data Timing

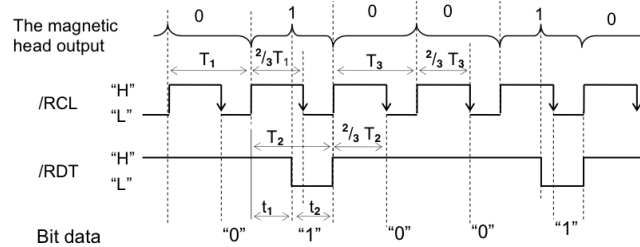
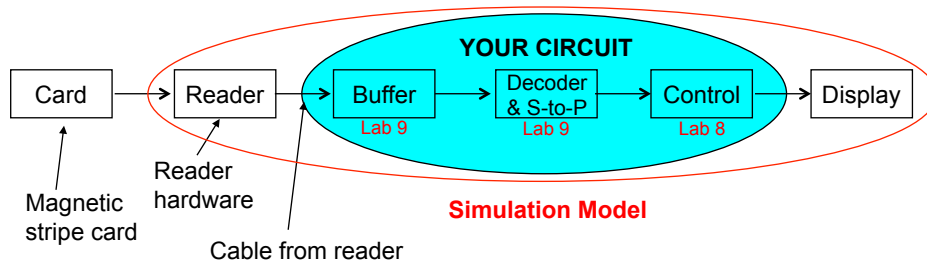


Fig 6.4 Timing sequence

Block diagram

- Major components
 - Reader outputs (simulation test fixture)
 - **Reader buffer, decoder, and serial-to-parallel converter (Lab 9)**
 - **LCD controller (Lab 8)**
 - LCD display (simulation test fixture)



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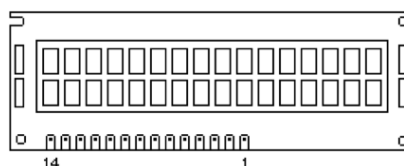
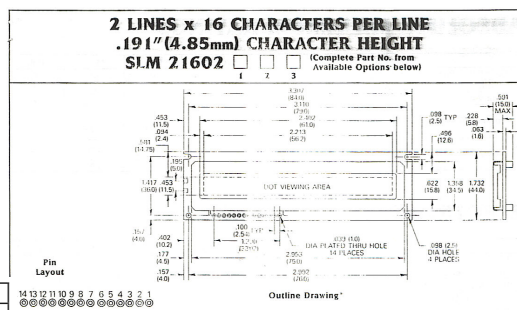
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LCD interface

- Eleven signal wires plus PWR/GND/ V_o
 - 1 mode input
 - 1 read/write control
 - 1 enable
 - 8 data lines (bi-directional)

Pin No	Name	I/O	Description
1	Vss	Power	GND
2	Vdd	Power	+5v
3	V _o	Analog	Contrast Control
4	RS	Input	Register Select
5	R/W	Input	Read/Write
6	E	Input	Enable (<i>Strobe</i>)
7	D0	I/O	Data <i>LSB</i>
8	D1	I/O	Data
9	D2	I/O	Data
10	D3	I/O	Data
11	D4	I/O	Data
12	D5	I/O	Data
13	D6	I/O	Data
14	D7	I/O	Data <i>MSB</i>



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8

LCD Operations

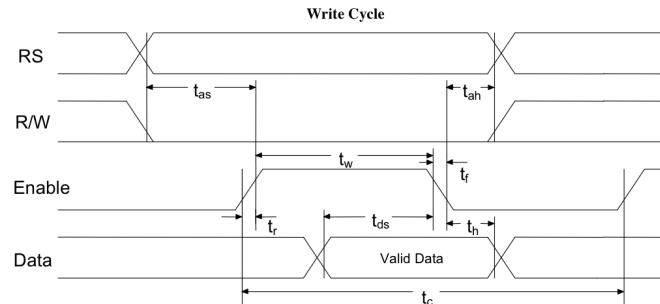
Instruction	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0	Description	Clocks
NOP	0	0	0	0	0	0	0	0	0	0	No Operation	0
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears display & sets address counter to zero.	165
Cursor Home	0	0	0	0	0	0	0	0	1	0	Sets address counter to zero, returns shifted display to original position. DDRAM contents remains unchanged.	3
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction, and specifies automatic shift.	3
Display Control	0	0	0	0	0	0	1	D	C	B	Turns display (D), cursor on/off (C) or cursor blinking (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shift display. DDRAM contents remains unchanged.	3
Function Set	0	0	0	0	1	DL	N	M	G	0	Sets interface data width(DL), number of display lines (N,M) and voltage generator control (G).	3
Set CGRAM Addr	0	0	0	1	Character Generator RAM						Sets CGRAM Address	3
Set DDRAM Addr	0	0	1	Display Data RAM Address						Sets DDRAM Address	3	
Busy Flag & Addr	0	1	BF	Address Counter						Reads Busy Flag & Address Counter	0	
Read Data	1	0	Read Data						Reads data from CGRAM or DDRAM	3		
Write Data	1	1	Write Data						Writes data from CGRAM or DDRAM	3		

Basic LCD operations

- Requires sequence of 4 instructions/commands on initialization (**RS = 0**)
 - **Command write (RW = 0)** – data bus pins carry command code
- Many more instructions/commands (**RS = 0**)
 - E.g., backup cursor, blink, etc. (look up appropriate DB values)
- Printing a character to the display (**RS = 1**)
 - **Data write (RW = 0)** – data bus pins carry character to display
- Read busy signal (on DB7)
 - LCD uses it to force a wait
 - **RW = 1**
 - Need to make sure not driving data lines (DB = 8'bzzzzzzzz)
 - Use DB7 as input, check if 0 (not busy) or 1 (busy)

Operation	RS	DB7...DB0
Clear Display	0	0000 0001
Function Set	0	0011 0011
Display On	0	0000 1100
Entry Mode Set	0	0000 0110
Write Character	1	DDDD DDDD

Timing details



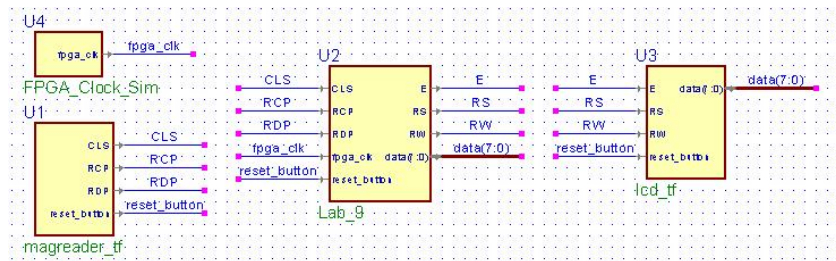
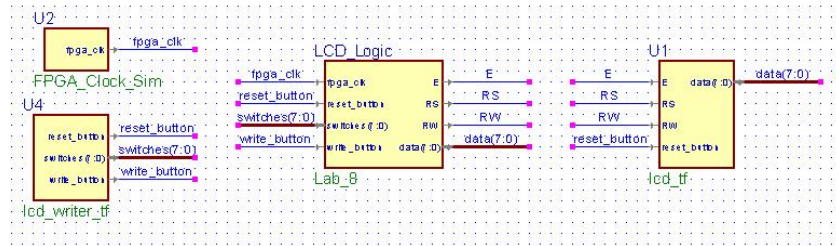
WRITE OPERATION					
Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{cyc E}$	1.0	—	—	μ s
Enable Pulse Width	PW E	450	—	—	ns
Enable Rise/Fall Time	t_{r,t_f}	—	—	25	ns
Address Set-up Time	t_{AS}	140	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Data Start-up Time	t_{DSW}	195	—	—	ns
Data Hold Time	t_{DH}	10	—	—	ns

ASCII codes

CHARACTER FONT DATA CODES

		UPPER 4-BIT HEXADECIMAL																
		0	1	2	3	4	5	6	7	A	B	C	D	E	F			
Higher 4-bit	Lower 4-bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111				
LOWER 4-BIT HEXADECIMAL	0	xxxx0000	00P	01P	02P	03P	04P	05P	06P	07P	08P	09P	0AP	0BP	0CP	0DP	0EP	0FP
	1	xxxx0001	00Q	01Q	02Q	03Q	04Q	05Q	06Q	07Q	08Q	09Q	0AQ	0BQ	0CQ	0DQ	0EQ	0FQ
	2	xxxx0010	00R	01R	02R	03R	04R	05R	06R	07R	08R	09R	0AR	0BR	0CR	0DR	0ER	0FR
	3	xxxx0011	00S	01S	02S	03S	04S	05S	06S	07S	08S	09S	0AS	0BS	0CS	0DS	0ES	0FS
	4	xxxx0100	00T	01T	02T	03T	04T	05T	06T	07T	08T	09T	0AT	0BT	0CT	0DT	0ET	0FT
	5	xxxx0101	00U	01U	02U	03U	04U	05U	06U	07U	08U	09U	0AU	0BU	0CU	0DU	0EU	0FU
	6	xxxx0110	00V	01V	02V	03V	04V	05V	06V	07V	08V	09V	0AV	0BV	0CV	0DV	0EV	0FV
	7	xxxx0111	00W	01W	02W	03W	04W	05W	06W	07W	08W	09W	0AW	0BW	0CW	0DW	0EW	0FW
	8	xxxx1000	00X	01X	02X	03X	04X	05X	06X	07X	08X	09X	0AX	0BX	0CX	0DX	0EX	0FX
	9	xxxx1001	00Y	01Y	02Y	03Y	04Y	05Y	06Y	07Y	08Y	09Y	0AY	0BY	0CY	0DY	0EY	0FY
	A	xxxx1010	00Z	01Z	02Z	03Z	04Z	05Z	06Z	07Z	08Z	09Z	0AZ	0BZ	0CZ	0DZ	0EZ	0FZ
	B	xxxx1011	00[01[02[03[04[05[06[07[08[09[0A[0B[0C[0D[0E[0F[
	C	xxxx1100	00\	01\	02\	03\	04\	05\	06\	07\	08\	09\	0A\	0B\	0C\	0D\	0E\	0F\
	D	xxxx1101	00]	01]	02]	03]	04]	05]	06]	07]	08]	09]	0A]	0B]	0C]	0D]	0E]	0F]
	E	xxxx1110	00^	01^	02^	03^	04^	05^	06^	07^	08^	09^	0A^	0B^	0C^	0D^	0E^	0F^
	F	xxxx1111	00_	01_	02_	03_	04_	05_	06_	07_	08_	09_	0A_	0B_	0C_	0D_	0E_	0F_

Block Diagrams for Labs 8 and 9



Purpose of the project

- Learn how to build a complete system that does something useful
- Read data sheets
- Use communicating state machines
- Use test fixtures and read some more complex Verilog code