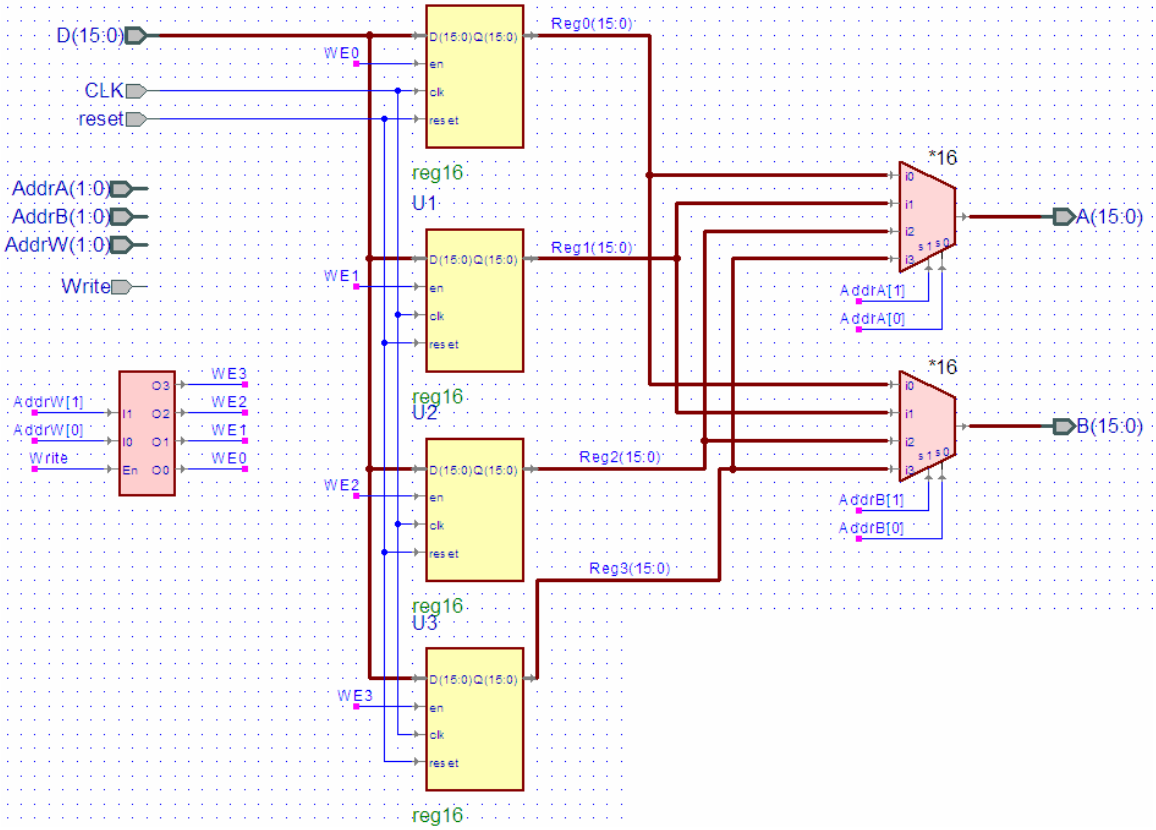
CSE 370 Homework 6 Solutions

1. Register File



2. Register File Test

Step	reset	R0	R1	R2	R3	Op code	AddrA	A	AddrB	B	AddrW	Result	Write
0	1	X	X	X	X	X	X	X	X	X	X	X	0
1	1	X	X	X	X	X	X	X	X	X	X	X	0
2	1	0	0	0	0	X	X	X	X	X	X	X	0
3	0	0	0	0	0	X	X	X	X	X	X	X	0
4	0	0	0	0	0	0	1	0	2	0	0	0	1
5	0	0	0	0	0	2	0	0	3	0	1	1	1
6	0	0	1	0	0	2	1	1	2	0	2	2	0
7	0	0	1	0	0	2	1	1	2	0	2	2	1
8	0	0	1	2	0	0	2	2	2	2	0	4	1
9	0	4	1	2	0	6	2	2	0	4	3	2	1
10	0	4	1	2	2	3	0	4	3	2	3	4	1
11	0	4	1	2	4	6	3	4	1	1	2	FFFD	1
12	0	4	1	FFFD	4	1	2	FFFD	3	4	0	FFF9	1

3. BCD Digit Counter

```
/*
        This BCD counter should count 0-9, then output
        a 1 on TC if the count rolls over to 0.  The reset
        of this module is a synchronous reset.
*/
module bcdCount ( clk ,reset ,cen ,count ,tc );

output [3:0] count ;
reg [3:0] count ;
output tc ;
wire tc ;

input clk ;
wire clk ;
input reset ;
wire reset ;
input cen ;
wire cen ;

// tc should be asserted if the count is currently 9
// and will be incremented on the next positive clock edge
assign tc = ((count == 4'h9) && cen);

// synchronous reset, only increment the count if cen is asserted
always @ (posedge clk) begin
        if (reset) begin
                count <= 4'h0;
        end
        else if (cen) begin
                if (count == 4'h9) begin
                        count <= 4'h0;
                end
                else begin
                        count <= count + 1'b1;
                end
        end
        else begin
                count <= count;
        end
end
endmodule
```