Lecture 11

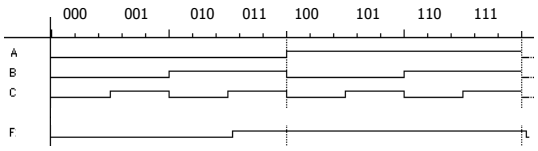
- Logistics
  - HW4 due on Wednesday
- Last lecture
  - PLDs
    - ROMs
  - Multilevel logic
- Today
  - Timing diagrams
  - Hazards

The "WHY" slide

- Timing diagram
  - Real gates have real delays and it is good to learn how to plot the information with respect to time.
- Hazards
  - Different delays can cause some output to get glitches. If these glitches are used in the next level of calculation, it could cause miscalculation. It is good to know when that happens and how to fix it.

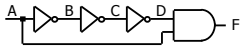
Timing diagram (aka waveforms)

- Shows time-response of circuits
- Can use as sideways truth table
- Example: F = A +BC



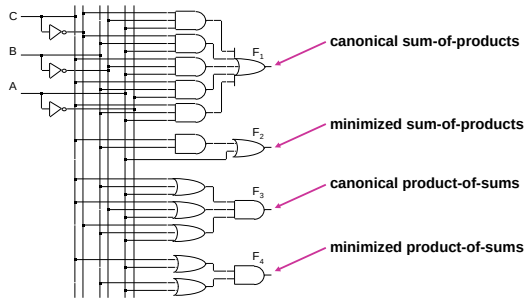
Timing diagrams

- Real gates have real delays
- Example: A' • A = 0
  - Delays cause transient F=1



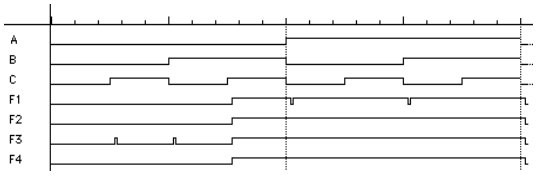
width of 3 gate delays

Example: F=A+BC in 2-level logic



Timing diagram for F = A + BC

- Time waveforms for F_1 – F_4 are identical
  - Except for timing hazards (glitches)



Hazards/glitches

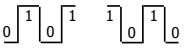
- Hazards/glitches: Undesired output switching
  - Occurs when different pathways have different delays
  - Wastes power (wire switching consumes power)
  - Causes circuit noise
  - Dangerous if logic makes a decision while output is unstable
- Solutions
  - Design hazard-free circuits
    - ⇨ Difficult when logic is multilevel
  - Wait until signals are stable

Types of hazards

- Static 1-hazard
  - Output should stay logic 1
  - Gate delays cause brief glitch to logic 0

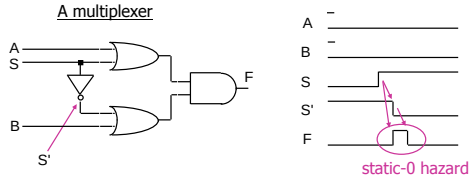
- Static 0-hazard
  - Output should stay logic 0
  - Gate delays cause brief glitch to logic 1

- Dynamic hazards
  - Output should toggle cleanly
  - Gate delays cause multiple transitions



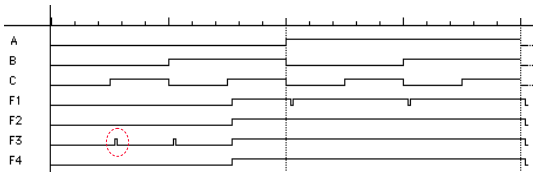
Static hazards

- Often occurs when a literal and its complement momentarily assume the same value
  - Through different paths with different delays
  - Causes an (ideally) static output to *glitch*

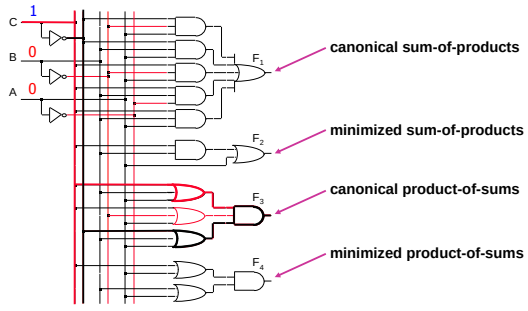


Timing diagram for F = A + BC

- Time waveforms for F_1 – F_4 are identical
  - Except for timing hazards (glitches)

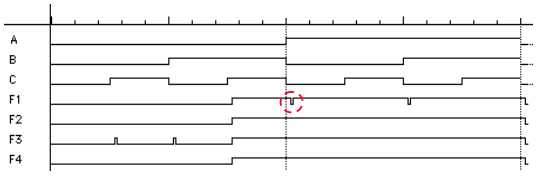


Example: F=A+BC in 2-level logic

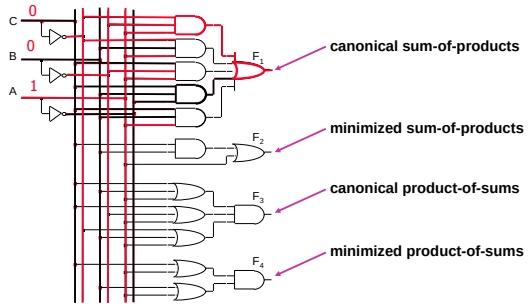


Timing diagram for F = A + BC

- Time waveforms for F_1 – F_4 are identical
  - Except for timing hazards (glitches)

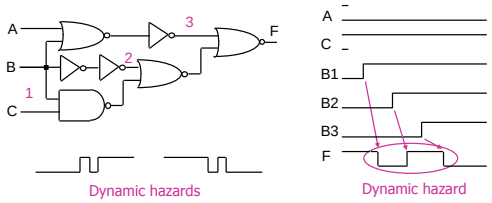


Example: F=A+BC in 2-level logic



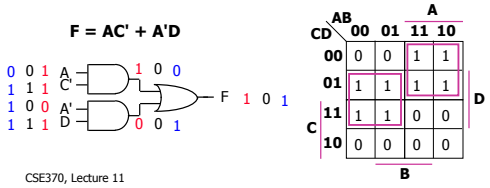
Dynamic hazards

- Often occurs when a literal assumes multiple values
  - Through different paths with different delays
  - Causes an output to toggle multiple times



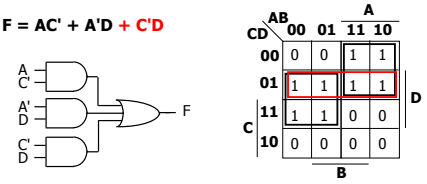
Eliminating static hazards (only in 2 level logic)

- Key idea: Glitches happen when a changing input spans separate K-map encirclements
  - Example: 1101 to 0101 change can cause a static-1 glitch



Eliminating static hazards (con't)

- Solution: Add redundant K-map encirclements
  - Ensure that all single-bit changes are covered by same block
  - First eliminate static-1 hazards: Use SOP form



- *If need to eliminate static-0 hazards, use POS form*

Summary of hazards

- We can eliminate static hazards in 2-level logic
  - For single-bit changes
  - Eliminating static hazards also eliminates dynamic hazards
- Hazards are a difficult problem
  - Multiple-bit changes in 2-level logic are hard
  - Static hazards in multilevel logic are harder
  - Dynamic hazards in multilevel logic are harder yet
- CAD tools and simulation/testing are indispensable