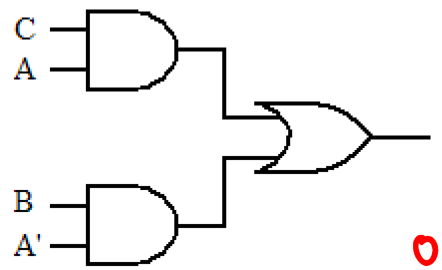
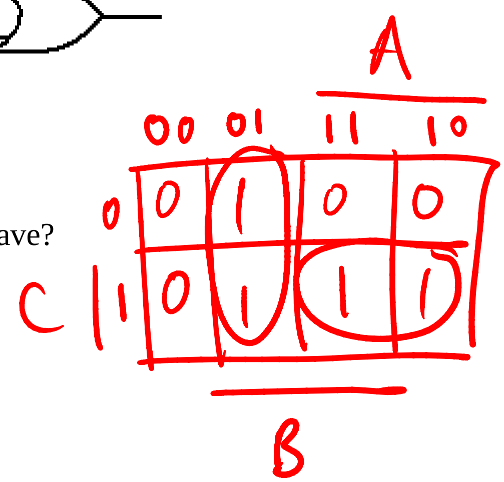
CSE 370 MIDTERM 2 SOLUTIONS Spring 2009

1. (15 points)



(a) What type of hazard does the above circuit have?

static-1

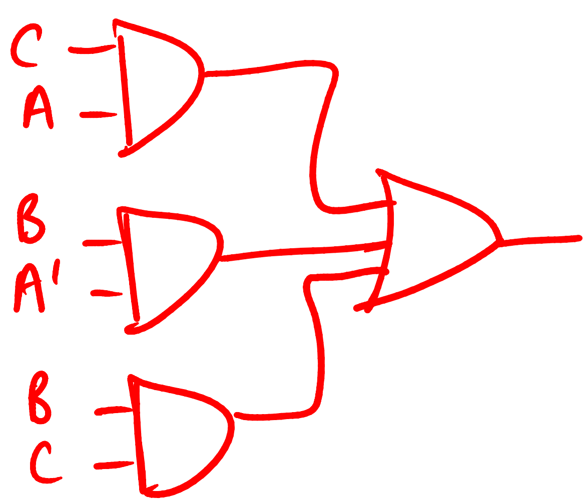


(b) Which input transitions (e.g., “From X to Y”) could potentially cause a glitch to occur?

011 to 111 (and vice versa)

It is incorrect to just say from A to A’.

(c) Redraw the circuit so that it is free of the hazard type answered in (a).



2. (15 points)

(a) Given the following K-map for a function F, write the minimized ***product-of-sums*** expression for F.

CD \ AB	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	X	0	0
10	0	1	1	X

$$(C+D)(B+D)(\bar{A}+\bar{C}+\bar{D})$$

(b) Which input transitions (e.g., “From X to Y”) could potentially cause a glitch to occur?

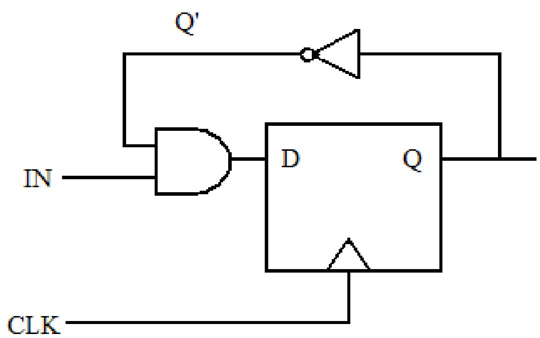
1011 to 1010 (and vice versa)

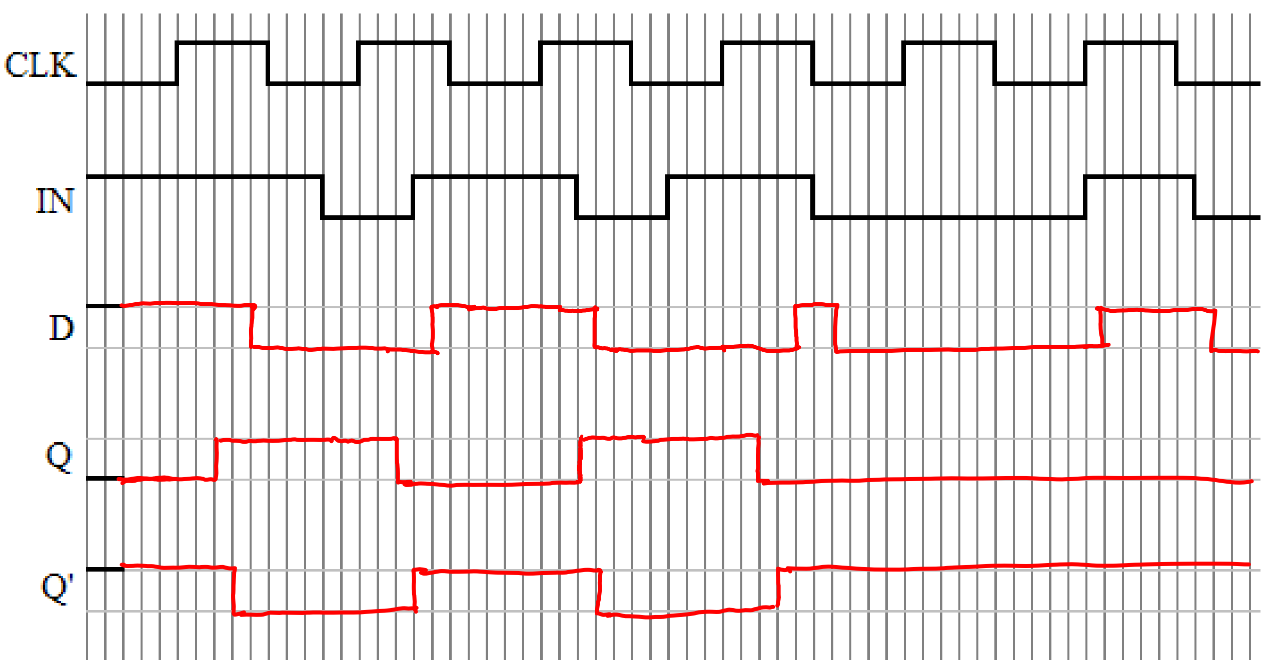
(c) Write a minimized ***product-of-sums*** expression for F that is free of static-0 hazards.

$$(C+D)(B+D)(\bar{A}+\bar{C}+\bar{D})(\bar{A}+B+\bar{C})$$

3. (35 points)

(a) Fill out the timing diagram for the following circuit. The clock period is 10 ns as marked on the diagram. Assume that the D flip-flop has no setup time, a 1 ns hold time, and a 2 ns propagation delay. The inverter and the AND gate have a gate delay of 1 ns each. As shown on the timing diagram, assume that all signal rise and fall times are instantaneous. The starting values for the wires and flip-flop are marked in the diagram.





(b) Write the state transition table for the circuit above.

IN	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	0

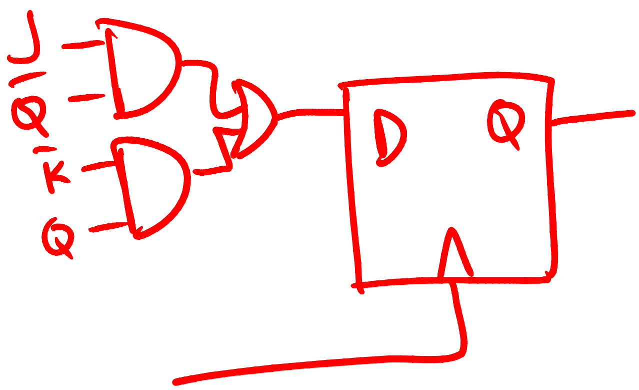
OR

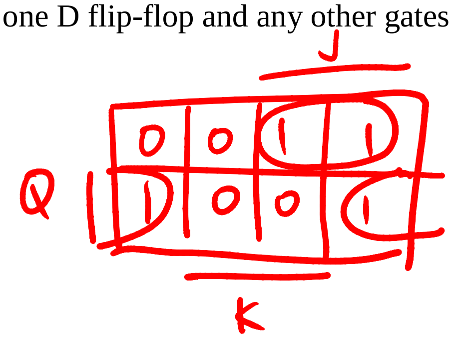
Q	IN	Q^+
0	0	0
0	1	1
1	0	0
1	1	0

4. (25 points)

J	K	Q	Q+	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

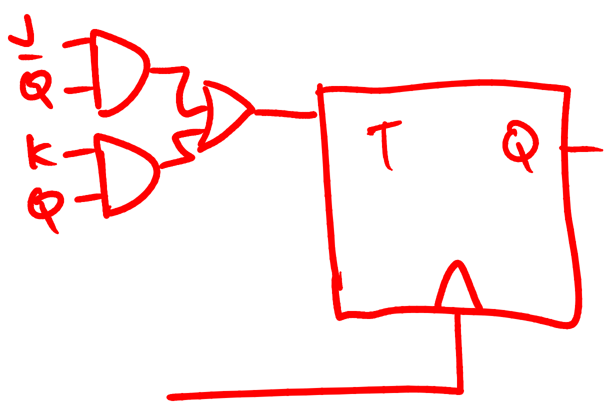
(a) Implement the state transition table above using one D flip-flop and any other gates you may need.

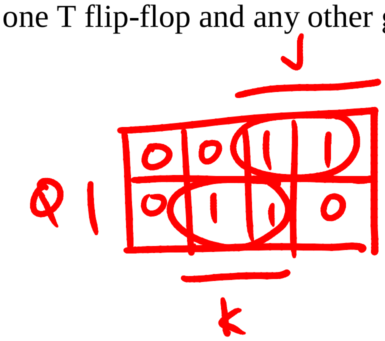




$J\bar{Q} + \bar{K}Q$

(b) Implement the state transition table above using one T flip-flop and any other gates you may need.





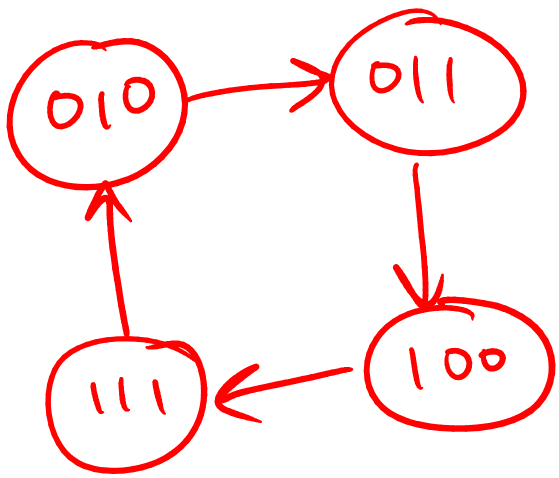
$J\bar{Q} + KQ$

5. (60 points) Build a counter that goes through the following sequence: 010 – 011 – 100 – 111 and then repeats.

(a) Show the following:

- (i) State diagram
- (ii) State transition table
- (iii) Minimized next-state functions
- (iv) Circuit implementation

(i) State diagram



(ii) State transition table

A	B	C	A^+	B^+	C^+
0	0	0	X	X	X
0	0	1	X	X	X
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	X	X	X
1	1	0	X	X	X
1	1	1	0	1	0

(iii) Minimized next-state functions

A^+

x	0	x	1
x	1	0	x

$\bar{B} + \bar{A}C$

B^+

x	1	x	1
x	0	1	x

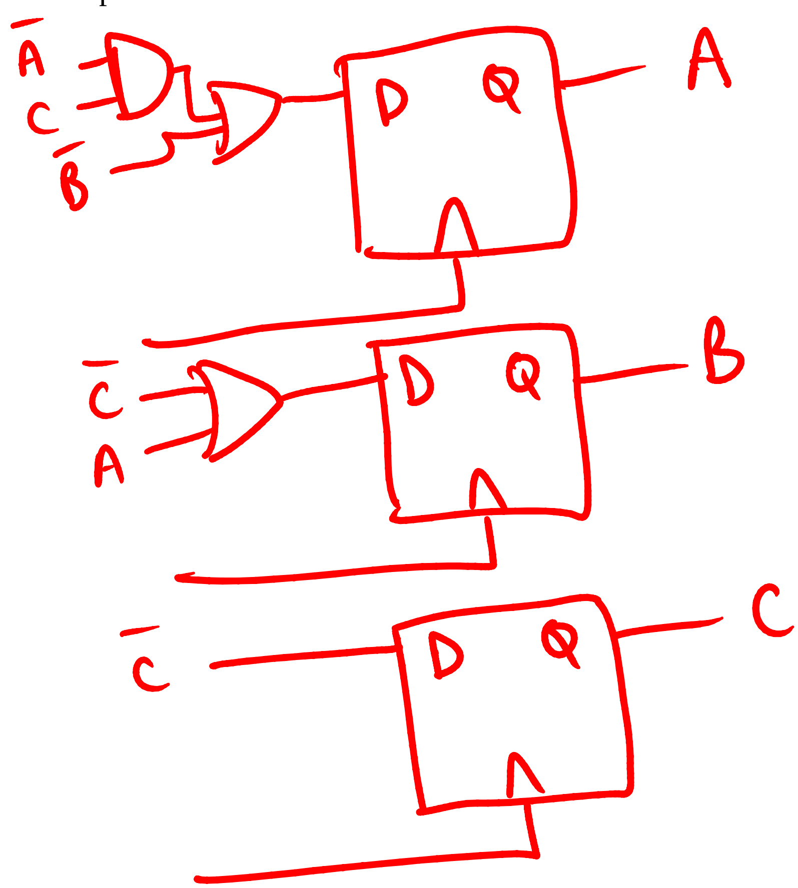
$\bar{C} + A$

C^+

x	1	x	1
x	0	0	x

$\bar{C}$

(iv) Circuit implementation



(c) Is the counter self-starting? Why or why not?

Yes. The non-counter states are 000, 001, 101, and 110. Based on our next-state functions, these states transition to 111, 100, 110, and 011 respectively. Thus, all non-counter states eventually reach valid counter states.