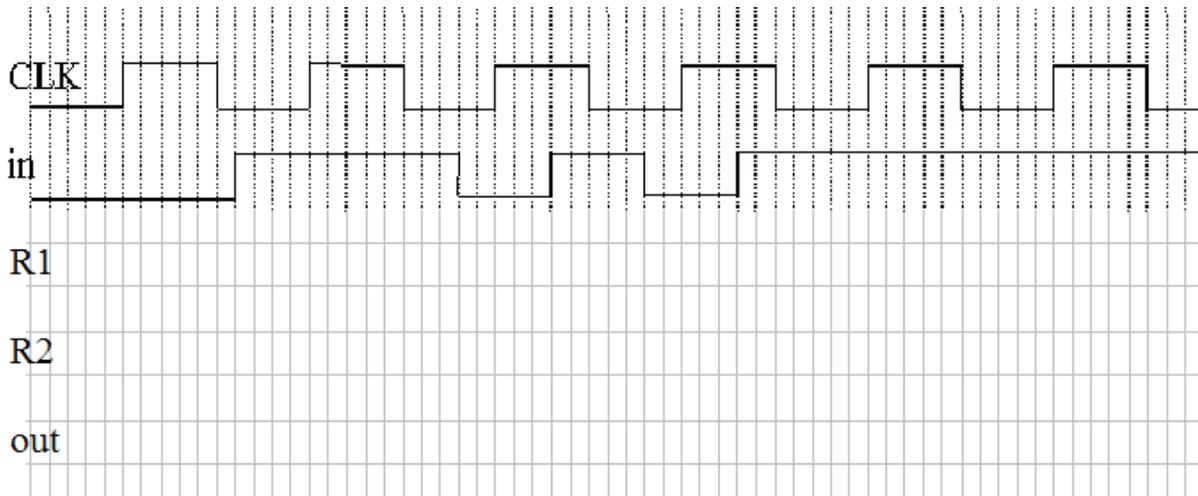
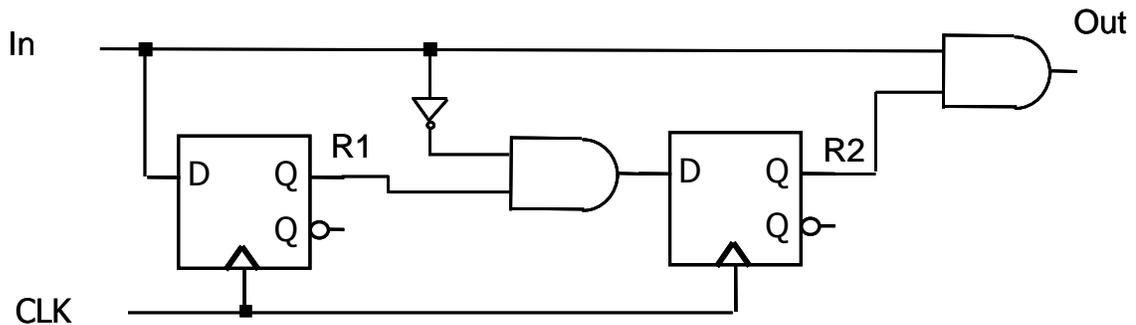


**Problem 1: (20 points)**

Fill out the timing diagram for the following circuit. The clock period is 10 ns as marked on the diagram. Assume that each D flip-flop has a propagation delay of 2 ns and hold time of 1 ns. Assume that each gate (inverter or AND) has a gate-delay of 1 ns. As shown on the timing diagram, assume that all signal rise and fall times are instantaneous.



**Problem 2: (10 points)**

Which of the following must always be true for proper operation of a sequence of identical flip-flops:

- (2 pts) (a) The set-up time cannot exceed the clock width?
- (2 pts) (b) The hold time must be less than propagation delay?
- (2 pts) (c) The clock period must be larger than the propagation delay plus the hold time?
- (2 pts) (d) The clock width must be larger than the propagation delay?
- (2 pts) (e) The set-up time plus the propagation delay must be less than the clock period?

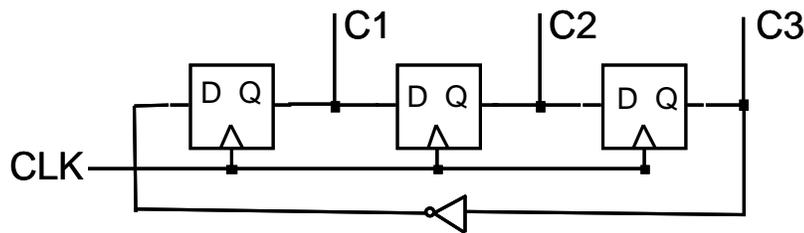
**Problem 3: (10 points)**

Given the following K-map for a function F, design a minimized sum-of-products for F that avoids static-1 hazards.

		<b>AB</b>		<b>A</b>	
		<b>00</b>	<b>01</b>	<b>11</b>	<b>10</b>
<b>CD</b>	<b>00</b>	0	0	X	0
	<b>01</b>	1	1	1	X
	<b>11</b>	0	1	1	0
	<b>10</b>	1	1	X	0
		<b>B</b>			
<b>C</b>		<b>D</b>			

**Problem 4: (20 points)**

(a) (12 points) Draw the complete state diagram for the following counter:



(b) (3 points) This counter is not self-starting. Why not?

(c) (5 points) How specifically would you change the state diagram to make this counter self-starting?

**(d) (5 points extra credit)** Show how to modify the circuit for this counter so that it will have the same functionality started from 000 but will implement your design change from part (c). Be sure to minimize your design.

**Problem 5: (40 points)**

In this problem you will build a 4-state cyclic counter with an additional single binary input. When the input is 1, the counter should increment by one; when it is 0, the counter should decrement by 1. There is also a separate Reset signal that returns the counter to value 0. To encode the states of your counter use the Gray Code encoding in which 0 is encoded as 00, 1 is encoded as 01, 2 is encoded as 11, and 3 is encoded as 10. (This will make your design simpler.) Your counter also should have a single output bit that is 1 if and only if the current value of your counter is 0; i.e., the difference between the number of 1's and 0's input since the last Reset signal is divisible by 4.

Show the following 4 steps:

- (i) Draw a state diagram of your counter and minimize it.
- (ii) Fill in a state transition table using the above encoding
- (iii) Minimize your logic using K-maps
- (iv) Implement your design as a circuit using D flip-flops having a separate Reset input.