

Lecture 4


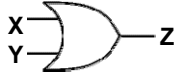
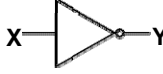

- ◆ Logistics
 - Classroom permanently changed to this one, EEB105
 - Lab2 is assigned today --- don't fall behind
 - HW1 is due on Wednesday in class before lecture
- ◆ Last lecture --- Boolean algebra
 - Axioms
 - Useful laws and theorems
 - Simplifying Boolean expressions
- ◆ Today's lecture
 - One more example of Boolean logic simplification
 - Logic gates and truth tables
 - Implementing logic functions

One more example of logic simplification

- ◆ Example:

$$Z = A'BC + AB'C' + AB'C + ABC' + ABC$$

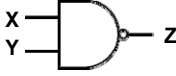



Logic gates and truth tables

◆ AND	$X \cdot Y$	XY		<table border="1"> <thead> <tr><th>X</th><th>Y</th><th>Z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	X	Y	Z	0	0	0	0	1	0	1	0	0	1	1	1
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◆ OR	$X + Y$			<table border="1"> <thead> <tr><th>X</th><th>Y</th><th>Z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	X	Y	Z	0	0	0	0	1	1	1	0	1	1	1	1
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◆ NOT	\bar{X}	X'		<table border="1"> <thead> <tr><th>X</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	0	1	1	0									
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◆ Buffer	X			<table border="1"> <thead> <tr><th>X</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td></tr> </tbody> </table>	X	Y	0	0	1	1									
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Logic gates and truth tables (con't)

◆ NAND	$\overline{X \cdot Y}$	\overline{XY}		<table border="1"> <thead> <tr><th>X</th><th>Y</th><th>Z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	Z	0	0	1	0	1	1	1	0	1	1	1	0
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◆ NOR	$\overline{X + Y}$			<table border="1"> <thead> <tr><th>X</th><th>Y</th><th>Z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	Z	0	0	1	0	1	0	1	0	0	1	1	0
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◆ XOR	$X \oplus Y$			<table border="1"> <thead> <tr><th>X</th><th>Y</th><th>Z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	Z	0	0	0	0	1	1	1	0	1	1	1	0
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Boolean expressions \Rightarrow logic gates

◆ Example: $F = (A \cdot B)' + C \cdot D$

A —
B —
C —
D —

◆ Example: $F = C \cdot (A + B)'$

A —
B —
C —

Truth tables \Rightarrow logic gates

◆ Given a truth table

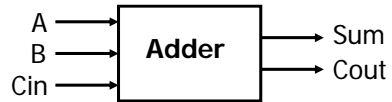
- Write the Boolean expression
- Minimize the Boolean expression
- Draw as gates
- Example:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Example: A binary full adder

◆ 1-bit binary adder

- Inputs: A, B, Carry-in
- Outputs: Sum, Carry-out



A	B	Cin	S	Cout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

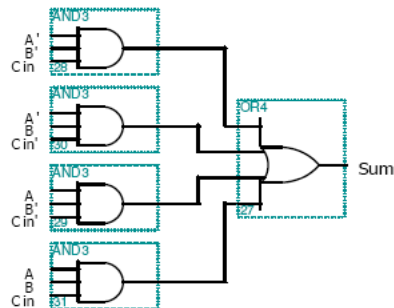
Sum =

Cout =

Full adder: Sum

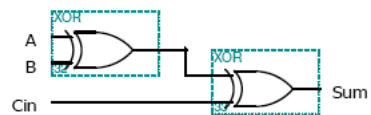
Before Boolean minimization

$$\text{Sum} = A'B'Cin + A'BCin' + AB'Cin' + ABCin$$



After Boolean minimization

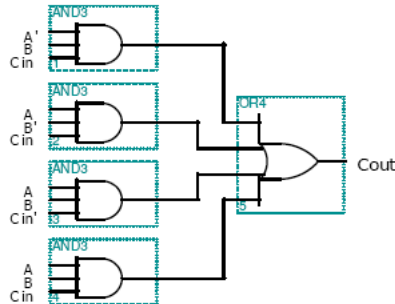
$$\text{Sum} = (A \oplus B) \oplus Cin$$



Full adder: Carry-out

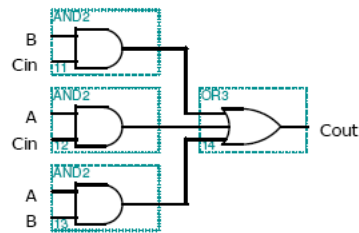
Before Boolean minimization

$$\text{Cout} = A'B\text{Cin} + AB'\text{Cin} + ABC\text{in}' + ABC\text{in}$$



After Boolean minimization

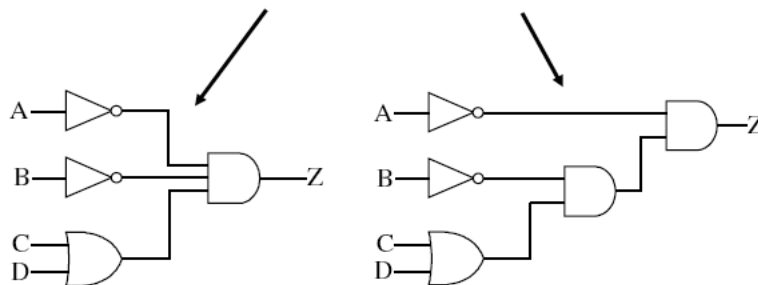
$$\text{Cout} = B\text{Cin} + A\text{Cin} + AB$$



Many possible mappings

◆ Many ways to map expressions to gates

■ Example: $Z = \bar{A} \cdot \bar{B} \cdot (C + D) = \bar{A} \cdot \bar{B} \cdot (C + D)$



What is the optimal gate realization?

- ◆ We use the axioms and theorems of Boolean algebra to “optimize” our designs
- ◆ Design goals vary
 - Reduce the number of gates?
 - Reduce the number of gate inputs?
 - Reduce number of chips and/or wire?
- ◆ How do we explore the tradeoffs?
 - CAD tools
 - Logic minimization: Reduce number of gates and complexity
 - Logic optimization: Maximize speed and/or minimize power

Minimal set

- ◆ We can implement any logic function from NOT, NOR, and NAND
 - Example: $(X \text{ and } Y) = \text{not } (X \text{ nand } Y)$
- ◆ In fact, we can do it with only NOR or only NAND
 - NOT is just NAND or NOR with two identical inputs

X	Y	X nor Y	X	Y	X nand Y
0	0	1	0	0	1
1	1	0	1	1	0

- NAND and NOR are duals: Can implement one from the other
 - ⚡ $X \text{ nand } Y = \text{not } ((\text{not } X) \text{ nor } (\text{not } Y))$
 - ⚡ $X \text{ nor } Y = \text{not } ((\text{not } X) \text{ nand } (\text{not } Y))$