

Overview

◆ Last lecture

- Introduction to sequential logic and systems
 - ↳ The basic concepts
 - ↳ A simple example

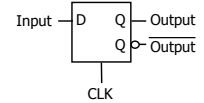
◆ Today

- Latches
- Flip-flops
 - ↳ Edge-triggered D
 - ↳ Master-slave
- Timing diagrams

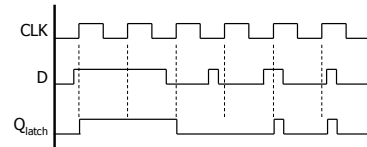
The D latch

◆ Output depends on clock

- Clock high: Input passes to output
- Clock low: Latch holds its output



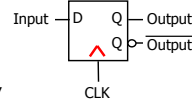
◆ Latches are level sensitive and transparent



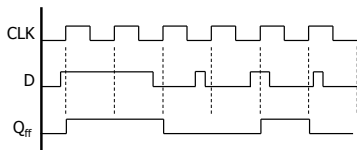
The D flip-flop

◆ Input sampled at clock edge

- Rising edge: Input passes to output
- Otherwise: Flip-flop holds its output

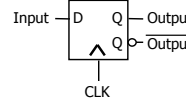


◆ Flip-flops are rising-edge triggered, falling-edge triggered, or master-slave

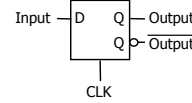


Terminology & notation

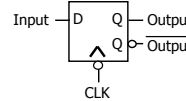
Rising-edge triggered D flip-flop



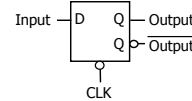
Positive D latch



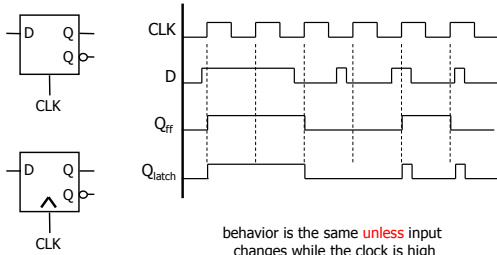
Falling-edge triggered D flip-flop



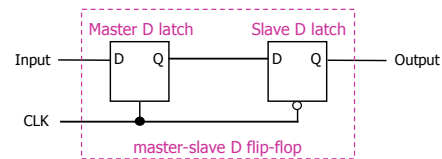
Negative D latch



Latches versus flip-flops



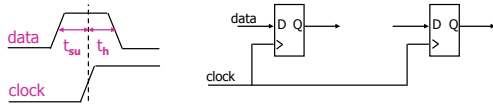
The master-slave D



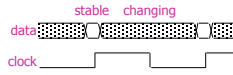
Class example: Draw the timing diagram

Flip-flop timing

- **Setup time t_{su}** : Amount of time the input must be stable before the clock transitions high (or low for negative-edge triggered FF)
- **Hold time t_h** : Amount of time the input must be stable after the clock transitions high (or low for negative-edge triggered FF)



There is a timing "window" around the clock edge during which the input **must** remain stable



Flip-flop timing (cont'd)

◆ Timing constraints

- Must meet setup and hold times
- Must meet minimum clock width
- Will have propagation delays (low to high & high to low)

