Lecture 11:
Multi-Level Logic

CSE 370, Autumn 2007
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Where We Are

• Last lecture: Quine-McCluskey Minimization
• This lecture: Multi-Level Logic
• Next lecture: Circuit Delay and Timing
• Homework 4 in progress
• Lab 3 done; lab 4 next week

2-Level Minimum Circuits are Not Always the Best Solution

• Important circuit metrics:
  • Size
  • Speed
  • Complexity
  • Energy efficiency
• How we approximate these metrics:
  • Number and kind of gates
  • Number of gate inputs
  • Circuit depth
Example: Full Adder Sum Output

More Extreme Example: 2-Bit Adder

No Simple Methods

- For 2-level minimization we have:
  - K-maps
  - Quine-McCluskey
  - Espresso
- For multi-level minimization we have:
  - Lots of heuristics
  - SIS
Factoring

- \( Z = ADF + AEF + BDF + BEF + CDF + CEF + G \)
  - AND: 6  OR: 1  Depth: 2
- \( Z = (AD + AE + BD + BE + CD + CE) \cdot F + G \)
  - AND: 7  OR: 6  Depth: 4
- \( Z = (AD + BD + CD + AE + BE + CE) \cdot F + G \)
  - AND: 7  OR: 6  Depth: 4
- \( Z = [A \cdot B \cdot C] + (A + B + CE) \cdot F + G \)
  - OR: 2  AND: 3  OR: 2  Depth: 5
- \( Z = (A + B + C) \cdot D + (A + B + C) \cdot E \)
  - OR: 1  OR: 2  AND: 1  Depth: 3

Using Multiplexors to Implement Functions

Cofactoring

- \( Z = ACE + A \cdot \neg C \cdot \neg D + \neg AB \cdot \neg E + \neg A \cdot \neg BD \)
- Cofactor A
- \( Z = A(CE + \neg C \cdot \neg D) + \neg A(\neg B \cdot \neg E + \neg BD) \)
- Cofactor C in the left expression and B in the right expression
- \( Z = A(CE) + \neg (\neg C \cdot \neg D) + \neg A(B \cdot \neg E + \neg BD) \)
Translating to Muxes

- A((C(E) + ¬C(¬D)) + ¬A(B(¬E) + ¬B(¬D)))

Thank You for Your Attention

- Start reading lab 4
- Start looking at homework 4
- Continue reading the book