For new designs, please refer to the PALCE22V10

PALC22V10D

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

- **Advanced second-generation PAL architecture**
- **Low power**
  - **— 90 mA max. commercial (10 ns)**
  - **— 130 mA max. commercial (7.5 ns)**
- **CMOS Flash EPROM technology for electrical erasability and reprogrammability**
- **Variable product terms**
  - **— 2 x(8 through 16) product terms**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**
- **Up to 22 input terms and 10 outputs**
- **DIP, LCC, and PLCC available**
  - **— 7.5 ns commercial version**
    5 ns t_{CO}
    5 ns t_S
    7.5 ns t_{PD}
    133-MHz state machine
  - **— 10 ns military and industrial versions**
    6 ns t_{CO}
    6 ns t_S
    10 ns t_{PD}
    110-MHz state machine
  - **— 15-ns commercial and military versions**
  - **— 25-ns commercial and military versions**
- **High reliability**
  - **— Proven Flash EPROM technology**

100% programming and functional testing

Functional Description

The Cypress PALC22V10D is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and the programmable macrocell.

The PALC22V10D is executed in a 24-pin 300-mil molded DIP, a 300-mil cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. The 22V10D can be electrically erased and reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as “registered” or “combinatorial.” Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through “array” configurable “output enable” for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

PALC22V10D features a variable product term architecture. There are 5 pairs of product term sums beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PAL C 22V10D is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

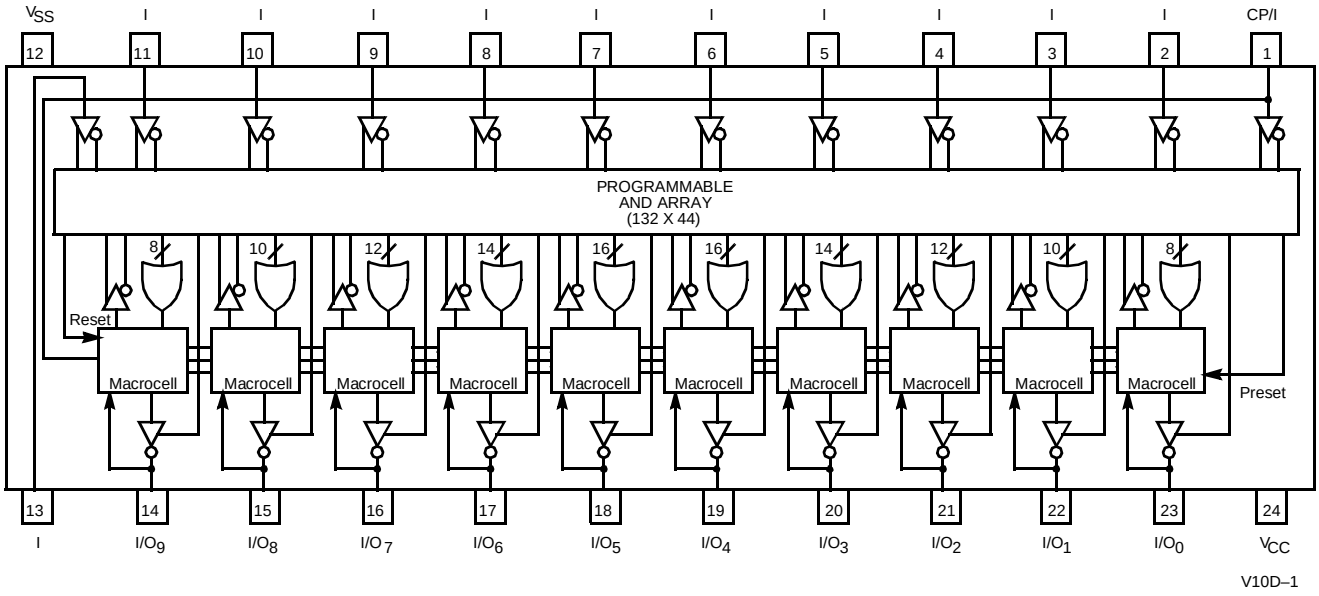
Additional features of the Cypress PALC22V10D include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets upon power-up.

The PALC22V10D, featuring programmable macrocells and variable product terms, provides a device with the flexibility to implement logic functions in the 500- to 800-gate-array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control state machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PALC22V10D provides lower-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

PAL is a registered trademark of Advanced Micro Devices

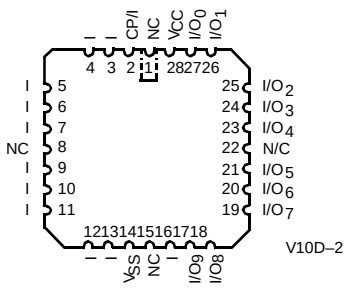
Logic Block Diagram (PDIP/CDIP)



V10D–1

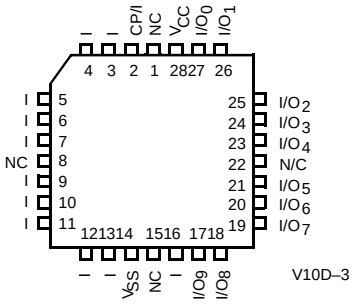
Pin Configuration

LCC
Top View



V10D–2

PLCC
Top View



V10D–3

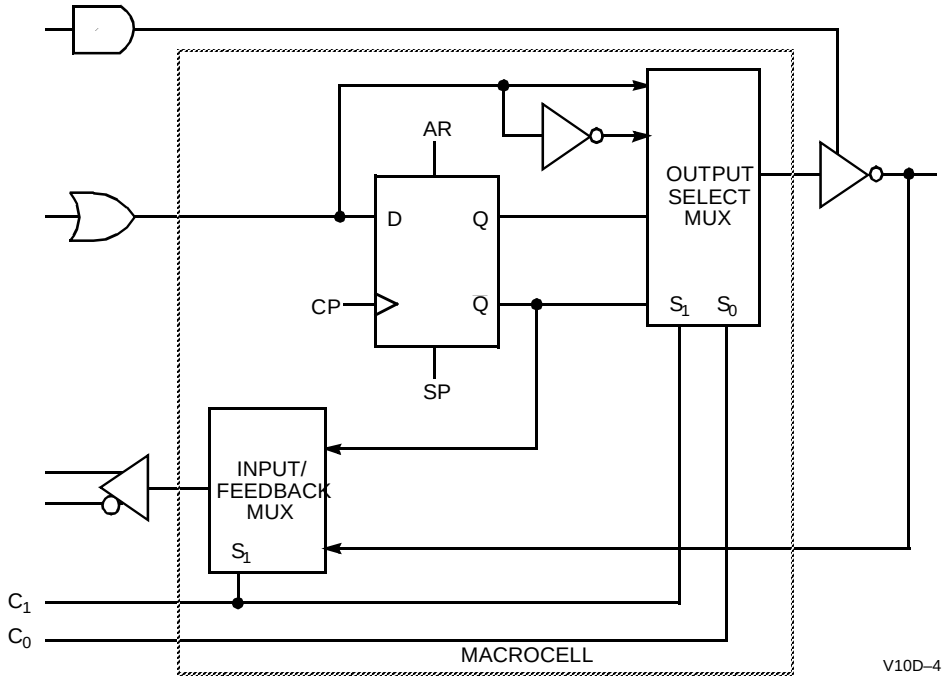
Configuration Table

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH

Configuration Table

Registered/Combinatorial		
C_1	C_0	Configuration
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +7.0V

DC Input Voltage..... -0.5V to +7.0V

Output Current into Outputs (LOW) .....16 mA

DC Programming Voltage 12.5V

Latch-Up Current..... >200 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Military[1]	–55°C to +125°C	5V ±10%
Industrial	–40°C to +85°C	5V ±10%

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.2 mA	Com'l	2.4		V
			I_{OH} = -2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}[2]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]			-0.5	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[5,6]			-30	-90	mA

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open in Unprogrammed Device	10, 15, 25 ns	Com'l		90	mA
			7.5 ns	Com'l		130	mA
			15, 25 ns	Mil/Ind		120	mA
			10 ns	Mil/Ind		120	mA
I_{CC2}[6]	Operating Power Supply Current	V_{CC} = Max., V_{IL} = 0V, V_{IH} = 3V, Output Open, Device Programmed as a 10-Bit Counter, f = 25 MHz	10, 15, 25 ns	Com'l		110	mA
			7.5 ns	Com'l		140	mA
			15, 25 ns	Mil/Ind		130	mA
			10 ns	Mil/Ind		130	mA

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to -3.0V for pulse durations less than 20 ns.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
6. Tested initially and after any design or process changes that may affect these parameters.

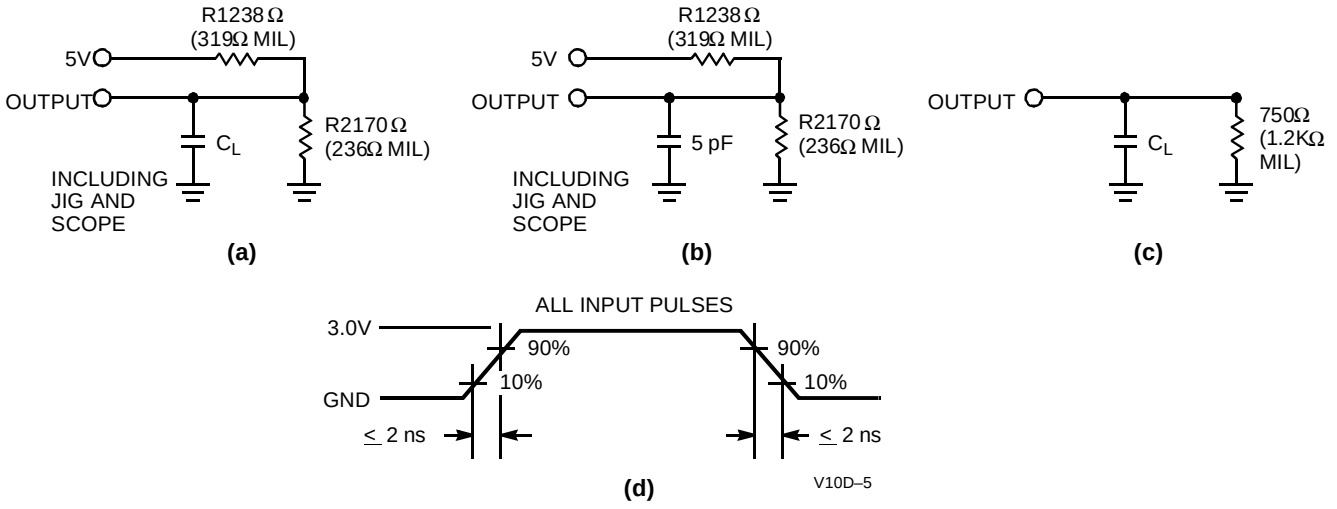
Capacitance[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

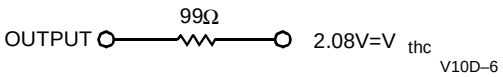
Endurance Characteristics[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

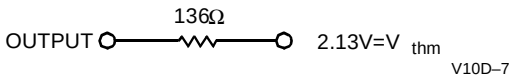
AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT(Commercial)



Equivalent to: THÉVENIN EQUIVALENT(Military)



Load Speed	C_L	Package
7.5, 10, 15, 25 ns	50 pF	PDIP, CDIP, PLCC, LCC

Parameter	V_X	Output Waveform Measurement Level
$t_{ER\ (-)}$	1.5V	 V10D–8
$t_{ER\ (+)}$	2.6V	 V10D–9
$t_{EA\ (+)}$	0V	 V10D–10
$t_{EA\ (-)}$	V_{thc}	 V10D–11

(e) Test Waveforms

Commercial Switching Characteristics PALC22V10D[2, 7]

Parameter	Description	22V10D-7		22V10D-10		22V10D-15		22V10D-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	7.5	3	10	3	15	3	25	ns
t_{EA}	Input to Output Enable Delay[10]		8		10		15		25	ns
t_{ER}	Input to Output Disable Delay[11]		8		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	2	5	2	7	2	8	2	15	ns
t_{S1}	Input or Feedback Set-Up Time	5		6		10		15		ns
t_{S2}	Synchronous Preset Set-Up Time	6		7		10		15		ns
t_H	Input Hold Time	0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	10		12		20		30		ns
t_{WH}	Clock Width HIGH[6]	3		3		6		13		ns
t_{WL}	Clock Width LOW[6]	3		3		6		13		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[12]	100		76.9		55.5		33.3		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 13]	166		142		83.3		35.7		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[6,14]	133		111		68.9		38.5		MHz
t_{CF}	Register Clock to Feedback Input[6, 15]		2.5		3		4.5		13	ns
t_{AW}	Asynchronous Reset Width	8		10		15		25		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		10		25		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		13		20		25	ns
t_{SPR}	Synchronous Preset Recovery Time	6		8		10		15		ns
t_{PR}	Power-Up Reset Time[6,16]	1		1		1		1		µs

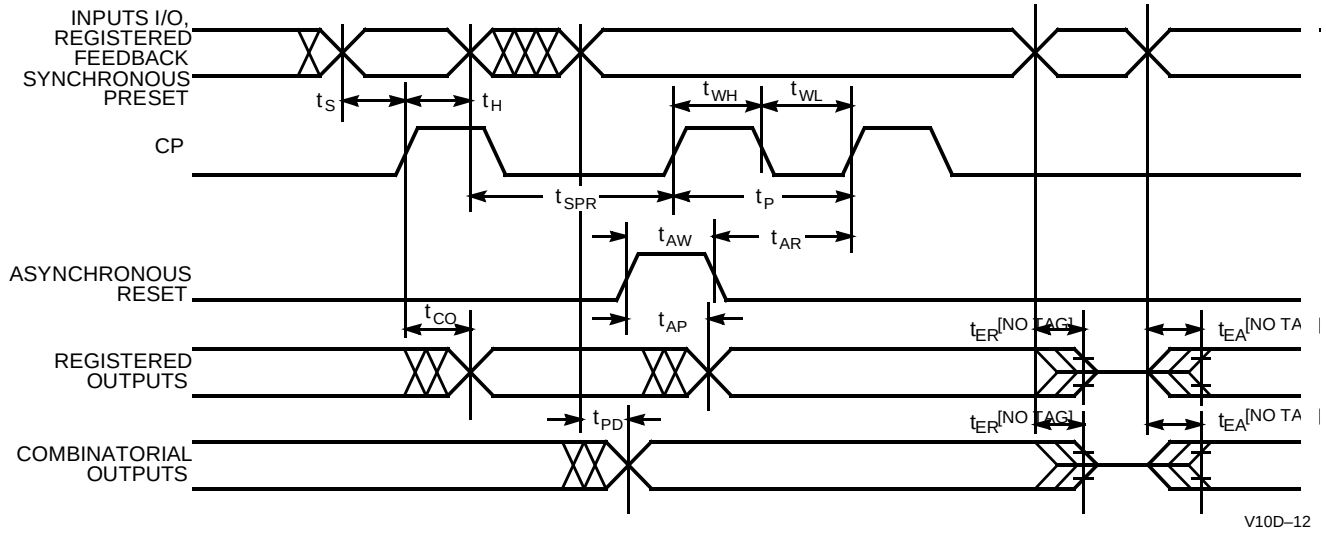
Notes:

7. Part (a) of AC Test Loads and Waveforms is used for all parameters except t_{ER} and $t_{EA(+)}$. Part (b) of AC Test Loads and Waveforms is used for t_{ER}. Part (c) of AC Test Loads and Waveforms is used for $t_{EA(+)}$.
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. The test load of part (a) of AC Test Loads and Waveforms is used for measuring $t_{EA(-)}$. The test load of part (c) of AC Test Loads and Waveforms is used for measuring $t_{EA(+)}$ only. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
11. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
15. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note above) minus t_S.
16. The registers in the PALC22V10D have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

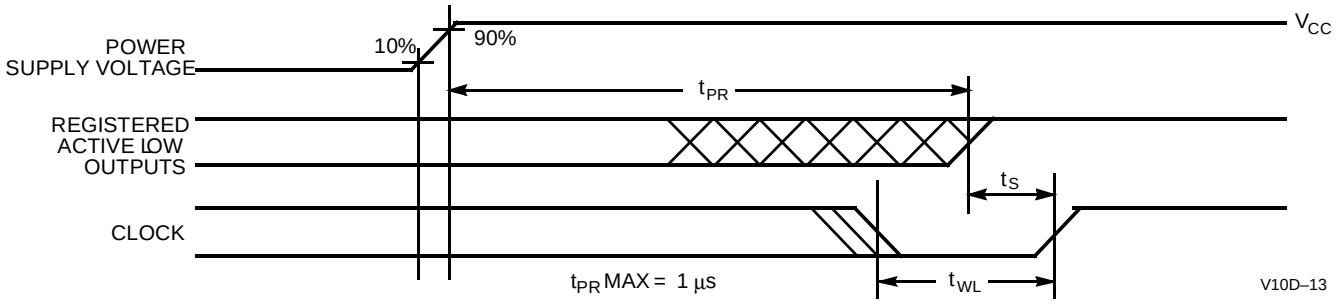
Military and Industrial Switching Characteristics PALC22V10D[2, 7]

Parameter	Description	22V10D-10		22V10D-15		22V10D-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	3	10	3	15	3	25	ns
t_{EA}	Input to Output Enable Delay[10]		10		15		25	ns
t_{ER}	Input to Output Disable Delay[11]		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	2	7	2	8	2	15	ns
t_{S1}	Input or Feedback Set-Up Time	6		10		18		ns
t_{S2}	Synchronous Preset Set-Up Time	7		10		18		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	12		20		33		ns
t_{WH}	Clock Width HIGH[6]	3		6		14		ns
t_{WL}	Clock Width LOW[6]	3		6		14		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[12]	76.9		50.0		30.3		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[6, 13]	142		83.3		35.7		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[6,14]	111		68.9		32.2		MHz
t_{CF}	Register Clock to Feedback Input[6,15]		3		4.5		13	ns
t_{AW}	Asynchronous Reset Width	10		15		25		ns
t_{AR}	Asynchronous Reset Recovery Time	6		12		25		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		20		25	ns
t_{SPR}	Synchronous Preset Recovery Time	8		20		25		ns
t_{PR}	Power-Up Reset Time[6, 16]	1		1		1		µs

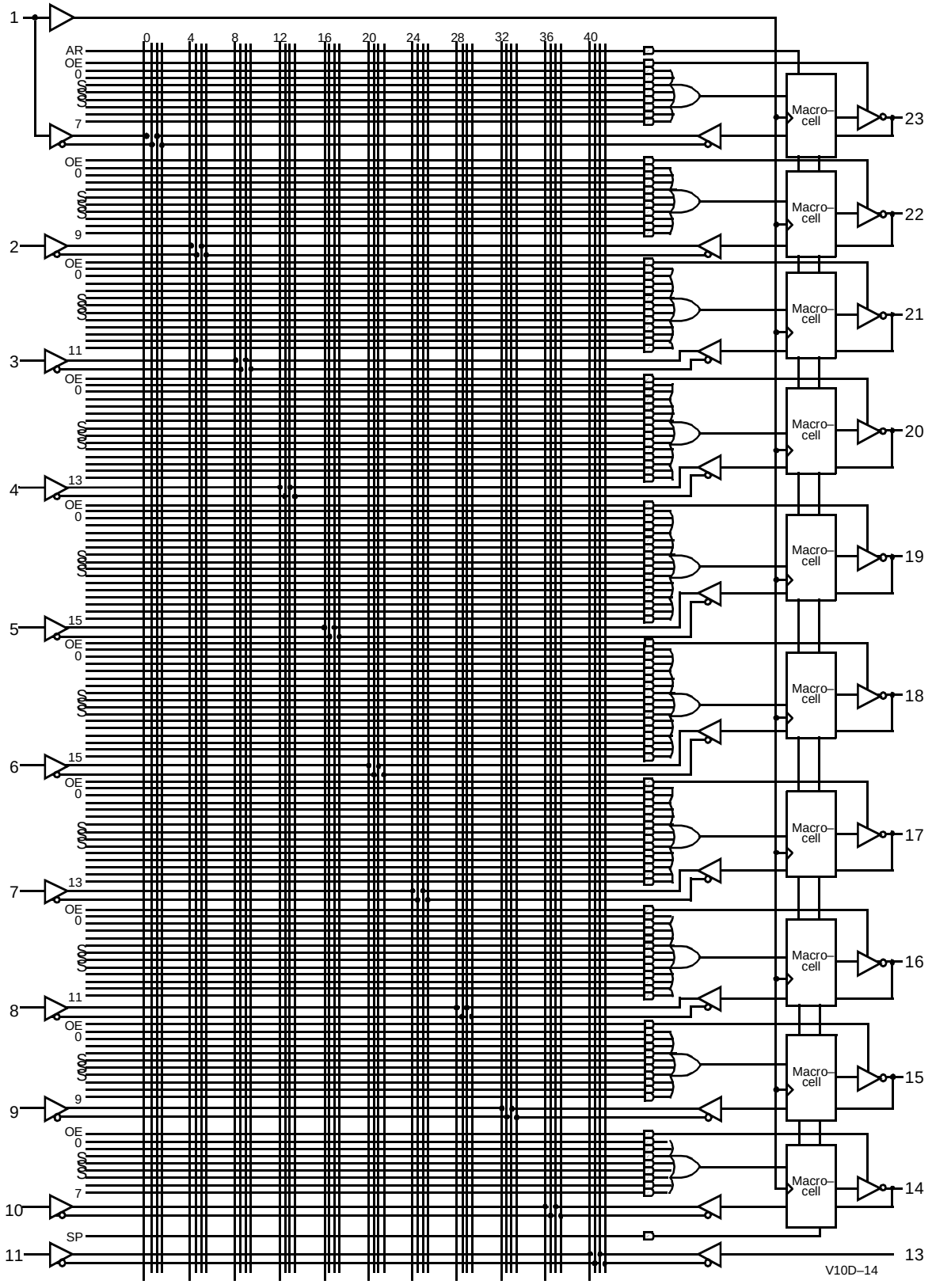
Switching Waveform



Power-Up Reset Waveform[16]



Functional Logic Diagram for PALC22V10D



Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
130	7.5	5	5	PALC22V10D-7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D-7PC	P13	24-Lead (300-Mil) Molded DIP	
90	10	6	7	PALC22V10D-10JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D-10PC	P13	24-Lead (300-Mil) Molded DIP	
150	10	6	7	PALC22V10D-10JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALC22V10D-10PI	P13	24-Lead (300-Mil) Molded DIP	
150	10	6	7	PALC22V10D-10DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10D-10KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D-10LMB	L64	28-Square Leadless Chip Carrier	
90	15	7.5	10	PALC22V10D-15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D-15PC	P13	24-Lead (300-Mil) Molded DIP	
120	15	7.5	10	PALC22V10D-15JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALC22V10D-15PI	P13	24-Lead (300-Mil) Molded DIP	
120	15	7.5	10	PALC22V10D-15DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10D-15KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D-15LMB	L64	28-Square Leadless Chip Carrier	
90	25	15	15	PALC22V10D-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PALC22V10D-25PC	P13	24-Lead (300-Mil) Molded DIP	
120	25	15	15	PALC22V10D-25JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
				PALC22V10D-25PI	P13	24-Lead (300-Mil) Molded DIP	
120	25	15	15	PALC22V10D-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10D-25KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10D-25LMB	L64	28-Square Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

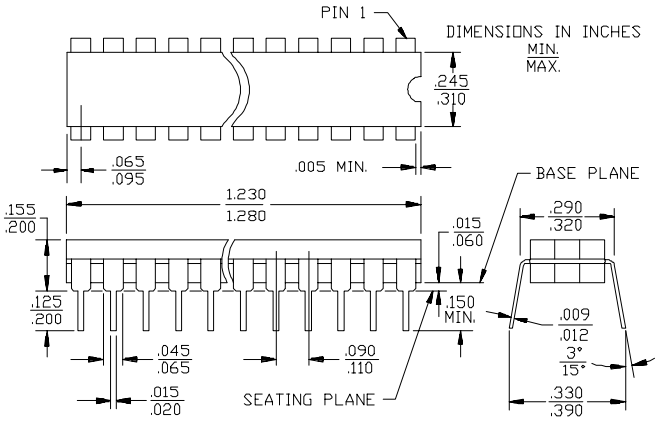
Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

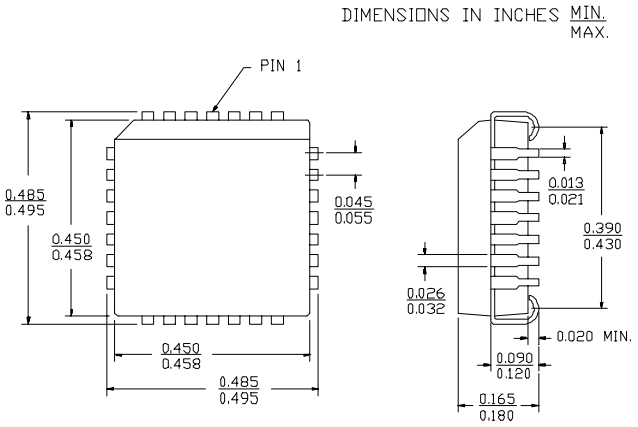
Document #: 38-00185-H

Package Diagrams

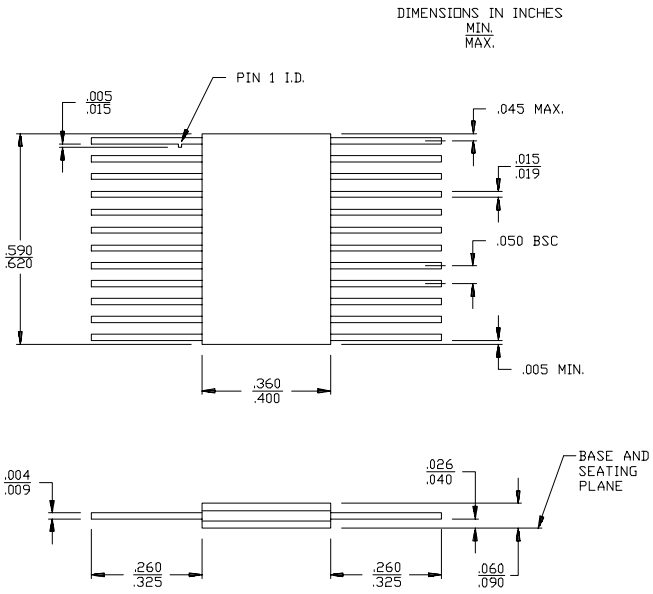
24–Lead (300–Mil) CerDIP D14
MIL-STD-1835 D-9 Config. A



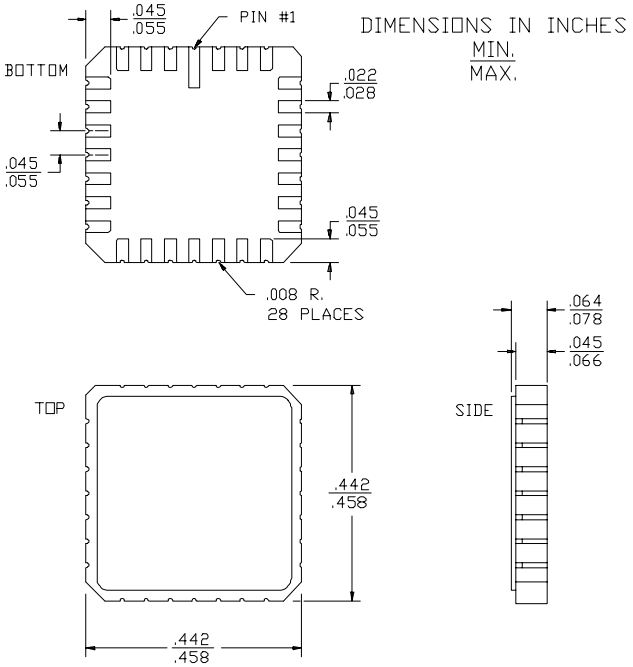
28–Lead Plastic Leaded Chip Carrier J64



24–Lead Rectangular Cerpack K73
MIL-STD-1835 F-6 Config. A

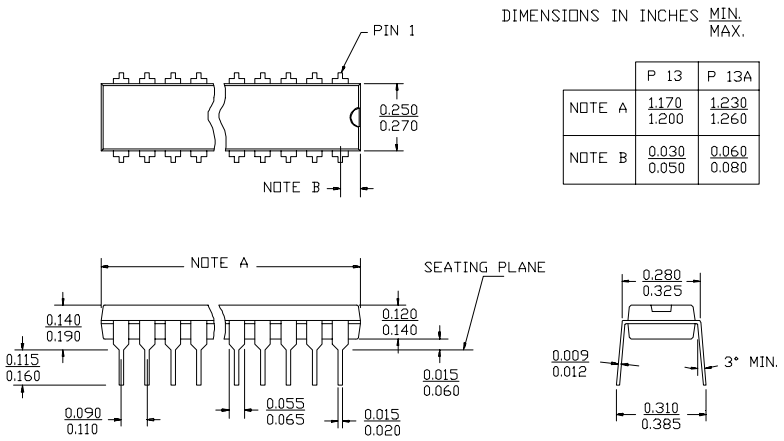


28–Square Leadless Chip Carrier L64
MIL-STD-1835 C-4



Package Diagrams (continued)

24–Lead (300–Mil) Molded DIP P13/P13A



DIMENSIONS IN INCHES MIN. / MAX.

	P 13	P 13A
NOTE A	1.170 / 1.200	1.230 / 1.260
NOTE B	0.030 / 0.050	0.060 / 0.080