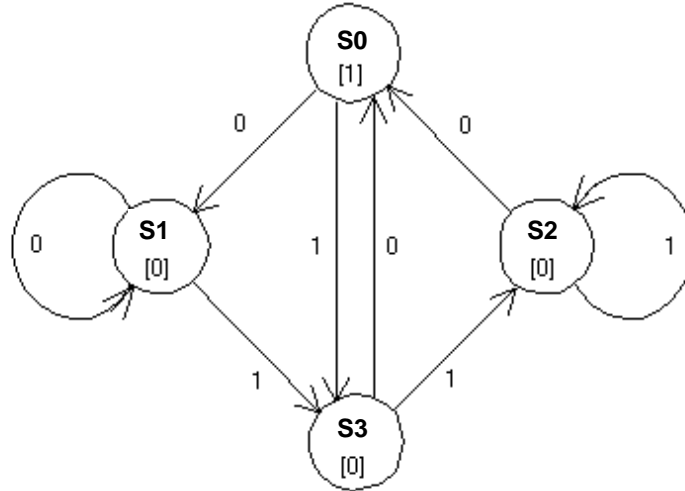


# CSE370 Quiz 5 (1 December)

Name \_\_\_\_\_

Given the state diagram below, with single input A and single output Z, show pseudo-Verilog code (clearly identifying any assign or always blocks) that specifies the same behavior. Implement the state transitions using an always block and the output using an assign statement.



```
module state_machine (A, Z, clk);
```

```
    input A;
    output Z;
    reg [ 0 : 1 ] state;
```

endmodule