HW #7 SOLUTIONS

7.10

7.12a) Let's use 1 bit up counter. Other solutions are also possible.
7.12b) 

This could affect the timing constraints of the circuit. For example, if we have 2 flip-flops cascaded together where flip-flop L is the flip-flop on the left and flip-flop R is the flip-flop on the right, the data out of L (A_L) must be settled and held according to the timing constraints of R. However, if flip-flop L has a long propagation delay, A_L may not be valid by the time the clock falls.
7.15 The case of 50% duty-cycle was analyzed in 7.14. The second case, 90% duty-cycle clock, changes the timing conditions of the circuits only slightly.

\[ T_{\text{period}} > T_{\text{pd}} + T_{\text{su}} \]

\[ 0.9 T_{\text{period}} > T_{\text{pd}} + T_{\text{su}} \]

\[ T_{\text{period}} > \frac{10}{9} (T_{\text{pd}} + T_{\text{su}}) \]

So, the period of the clock must become slightly larger to accommodate the propagation delay and setup time under the new duty cycle.