1. **CLD-II, Chapter 6, problem 6.10, all parts.**

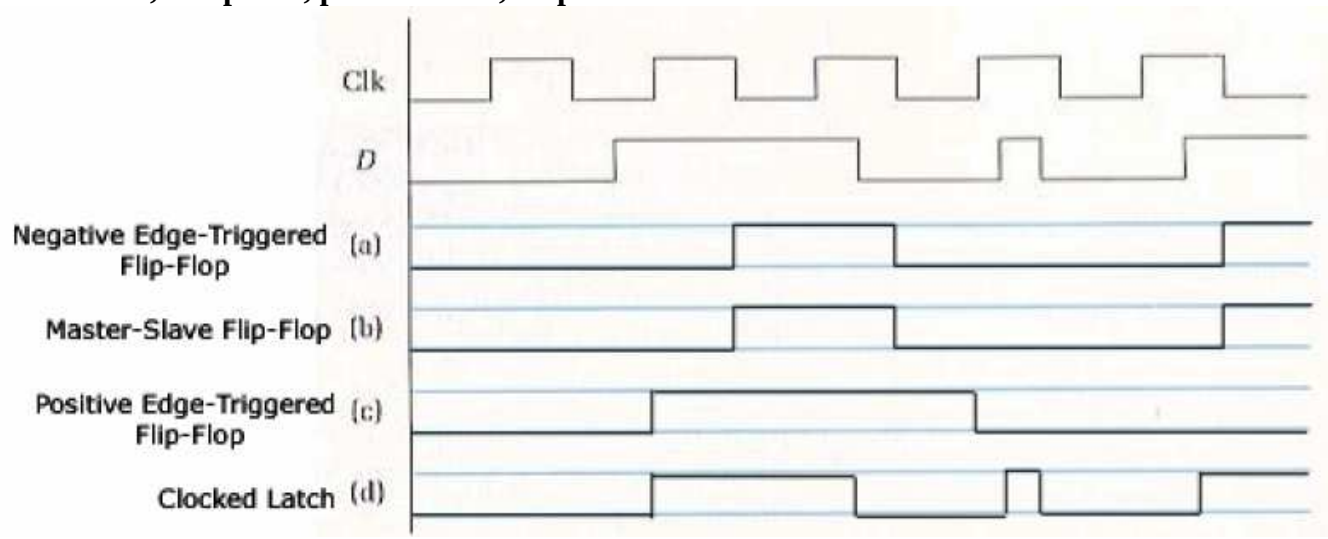

Figure 1

2. **CLD-II, Chapter 6, problem 6.11, all parts.**
   Identify the following statements as either true or false:

   (a) The inputs to a level-sensitive latch always affect its output.

   False, they only affect the output when the clock is asserted. (see pages 266 – 268).

   (b) Flip-flop delays from the change in the clock edge to the change in the output typically are shorter than flip-flop hold times, so shift registers can be constructed from cascaded flip-flops.

   False, propagation delay (which is the delay between the time when the clock is asserted and the output is valid) needs to be longer than the hold times otherwise we wouldn't be able to cascade flip-flops (e.g. the input values cannot change during the hold times). (see pages 276 – 281).

   (c) Assuming zero setup and hold times, clocked latches and flip-flops produce the same outputs as long as the inputs do not change while the clock is asserted.

   True (see pages 266 – 267, 275 – 276)
   False was also accepted because if we have a negative-edge triggered flip-flop and a positive clock triggered latch, we can get a different output by changing the output when the clock is low. However, the better answer is true because the problem states that the the clock is asserted. If we have a negative-edge triggered flip flop, we should have a latch triggered when the clock is low (asserted).

   (d) A master-slave flip-flop behaves similarly to a clocked latch, except that its output can change only near the rising edge of the clock.

   False, its output changes only near the falling edge of the clock. (see pages 269 – 270).

(e) An edge-triggered D flip-flop requires more internal gates than similar device constructed from a J-K master-slave flip flop.

False, the J-K master-slave flip-flop requires more gates. (see page 271).

3. CLD-II, Chapter 6, problem 6.18
Given the timing specification of the 74LS74 filp-flop of Figure 6.30, what is the worst-case skew in the clock that could be tolerated when one 74LS74 needs to pass its value to another 74LS74, as in Figure 6.33?

From the diagram, we learn the following:
$T_h = 0.5$ ns
$T_p = 1.1 – 3.6$ ns (depending on environmental conditions)

Since the propagation delay can vary, we must assume the worst case scenario. Using the equation on page 281:

$T_p > T_{skew} + T_h$
$T_{skew} < T_p – T_h$

The smaller the propagation delay, the smaller our skew is allowed to be, so we must assume that T_p is 1.1ns.

$T_{skew} < 1.1$ ns $– 0.5$ ns
$T_{skew} < 0.6$ ns

Several people used 3.6 ns for T_p in order to maximize T_{skew}, but this does not ensure correct operation in all environments.