2 LINES x 16 CHARACTERS PER LINE
.191" (4.85mm) CHARACTER HEIGHT
SLM 21602 ☐ ☐ ☐

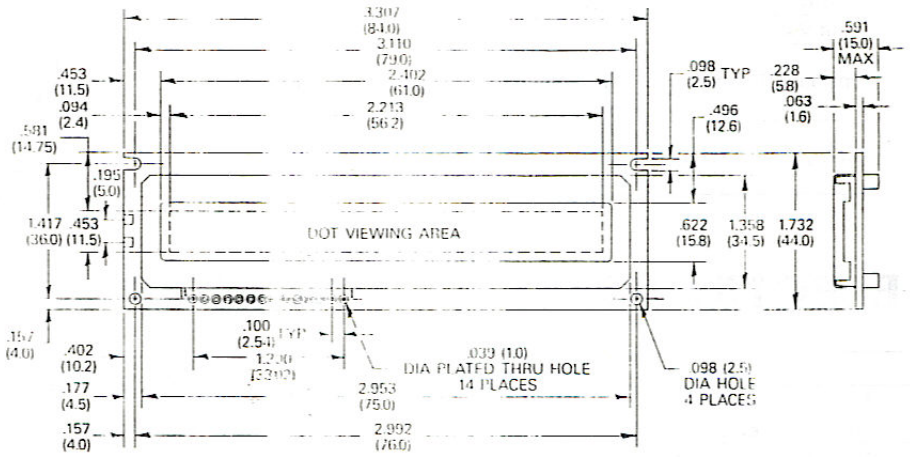
(Complete Part No. from Available Options below)

1 2 3

Pin Layout

14 13 12 11 10 9 8 7 6 5 4 3 2 1

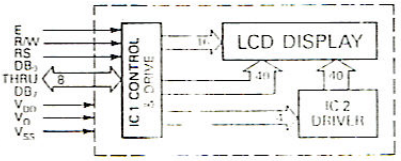
Outline Drawing*



Interface Pin Connections

Pin No.	Symbol	Function	
1	V_{SS}	0V	Power supply
2	V_{DD}	+5V	
3	V_O	--	
4	RS	H: Data input L: Instruction input	
5	R/W	H: Read(MPU←LCM) L: Write(MPU→LCM)	
6	E	Enable signal	
7	DB0		Data bus line
8	DB1		
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		

Block Diagram



Available Options

1. Viewing Angle:
   - B — Bottom
   - T — Top
2. Fluid Type:
   - S — Commercial (0°C to +50°C)
   - H — Industrial (-20°C to +70°C)
   - W — Wide Viewing Cone (0°C to +50°C)
3. Viewing Mode:
   - A — Reflective Positive Image/no lamp
   - B — Transflective Positive Image/with EL lamp
   - E — Transmissive Negative Image/with EL lamp

Voltage Requirements

Optimum Power Supply Voltage (V_{DD}-V_O)
Units: Volts ± 0.1V

Commercial Fluid			Industrial Fluid			Wide Viewing Cone Fluid		
0°C T_{OP}	+25°C T_{OP}	+50°C T_{OP}	-20°C T_{OP}	+25°C T_{OP}	+70°C T_{OP}	0°C T_{OP}	+25°C T_{OP}	+50°C T_{OP}
@ 1/16 Duty Cycle								
4.7	4.4	3.7	8.9	8.0	6.5	8.0	6.8	5.8

See Power Supply Schematics on page 36.

Display Pattern*

5x7 + Cursor Format

(Character Pitch = .140 in.)

Reference Information

	Page
Ordering Information	4
Viewing Mode Description Chart	4
Absolute Maximum Ratings	36
Electrical Specifications	36
Viewing Angle Diagram	36
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Display Data Address Chart	42
EL Lamp Inverters	46

*All dimensions in inches (mm). Drawings not to scale. All specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Min.	Max.	Unit
Logic Circuit Power Supply Voltage		V_{DD}-V_{SS}	0	7.0	V
LC Driver Circuit Supply Voltage		V_{DD}-V_O	0	13.5	V
Input Voltage		V_I	V_{SS}	V_{DD}	V
Operating Temperature	Commercial fluid Wide viewing cone fluid	t_a	0	+50	°C
	Industrial fluid		-20	+70	
Storage Temperature	Commercial fluid Wide viewing cone fluid	t_{stg}	-20	+70	°C
	Industrial fluid		-40	+90	

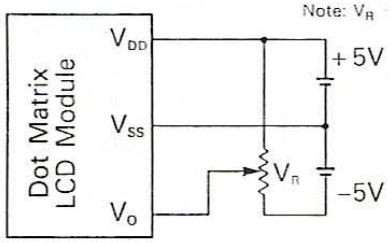
ELECTRICAL SPECIFICATIONS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High Input Level Voltage	V_{IH}	—	2.2	—	—	V
Low Input Level Voltage	V_{IL}	—	—	—	0.6	V
High Output Level Voltage	V_{OH}	$-I_{OH}$ = 0.2 mA	2.4	—	—	V
Low Output Level Voltage	V_{OL}	I_{OL} = 1.2mA	—	—	0.4	V
Power Current	I_{DD}	V_{DD} = 5.0 V	—	0.8	2.0	mA

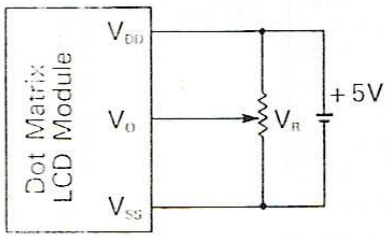
POWER SUPPLY SCHEMATICS

See individual module specification pages for voltage settings to obtain optimum contrast and viewing angle.

Note: V_R = Variable Resistor 10 KΩ to 20 KΩ



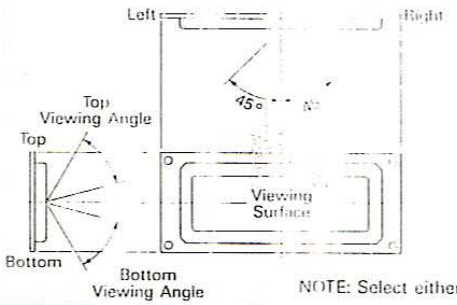
For Modules With Industrial Temperature Range Fluid or Wide Viewing Cone Fluid (Type H or W)



For Modules With Commercial Temperature Range Fluid (Type S)

VIEWING ANGLE DIAGRAM

Viewing Angle (All LCDs)



NOTE: Select either top or bottom viewing angle

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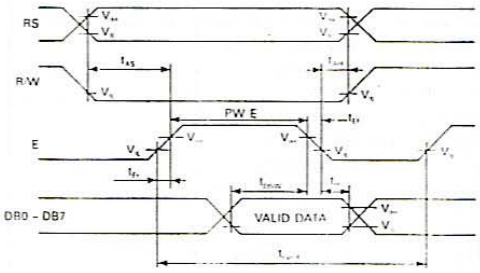
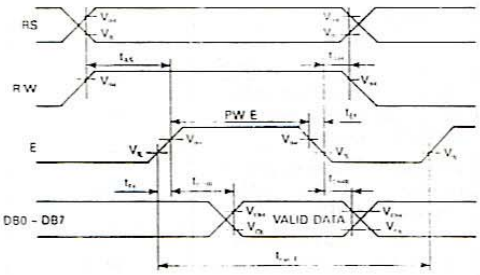
TIMING CHARACTERISTICS



WRITE OPERATION					
Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{cyc\,E}$	1.0	—	—	μs
Enable Pulse Width	PW E	450	—	—	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	—	—	25	ns
Address Set-up Time	t_{AS}	140	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Data Start-up Time	t_{DSW}	195	—	—	ns
Data Hold Time	t_{H}	10	—	—	ns



READ OPERATION					
Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{cyc\,E}$	1.0	—	—	μs
Enable Pulse Width	PW E	450	—	—	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	—	—	25	ns
Address Set-up Time	t_{AS}	140	—	—	ns
Address Hold Time	t_{AH}	10	—	—	ns
Data Delay Time	t_{DDR}	—	—	320	ns
Data Hold Time	t_{DHR}	20	—	—	ns

PIN FUNCTION CHART

Pin Name	I/O	Function
V_{SS}	—	Ground; 0V
V_{DD}	—	+5 V
V_O	—	Power supply for LC driving
RS	I	Signal to select registers "0": Instruction register (for write) Busy flag; address counter (for read) "1": Data register (for read and write)
R/W	I	Signal to select read (R) and write (W) "0": Write MPU → LCD Module "1": read MPU ← LCD Module
E	I	Operation start signal for data read or write
DB0 thru DB3	I/O	Data bus of lower order 4 lines having bidirectional tri-state. Used for data transfer between the MPU and the module. These four are not used during 4-bit operation
DB4 thru DB7	I/O	Data bus of higher order 4 lines having bidirectional tri-state. Used for data transfer between the MPU and the module. DB7 can be used as a BUSY flag.

NOTE: In the module, the data can be sent in either 4-bit 2-sequence operation or 8-bit single-operation so that it can interface to both 4 and 8-bit MPU's.

1. When interface data is 4 bits long, data is transferred using only line DB4~DB7 and DB0~DB3 are not used. Data transfer between the module and the MPU is complete when the 4-bit data is transferred twice. Data of the higher order 4 bits (the contents of DB4~DB7 when the interface data is 8 bits long) is transferred first, and the lower order 4 bits (the contents of DB0~DB3 when the interface data is 8 bits long) follows.
2. When the interface data is 8 bits long, data is transferred using all 8 data lines of DB0 ~ DB7.

INSTRUCTION CODES

Instruction	Set		Instruction Code								Description	Execution Time (when f_{cp} or f_{osc} is 250KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0)	82 μs –1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 μs –1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D). Cursor ON/OFF (C), and blink of cursor position character (B).	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						5Sets the CG RAM address CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address DD RAM data is sent and received after this setting	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs
	I/D = 1: Increment S = 1: Accompanies display shift S/C = 1: Display shift R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits N = 1: 2 lines F = 1: 5x10 dots BF = 1: Internally operating BF = 0: Can accept instruction D = 0: Display OFF C = 0: Cursor OFF B = 0: Blink OFF										I/D = 0: Decrement S/C = 0: Cursor move DL = 0: 4 bits N = 0: 1 line F = 0: 5x7 dots D = 1: Display ON C = 1: Cursor ON B = 1: Blink ON	DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address Corresponds to cursor address AC: Address counter used for both of DD and CG RAM address	Execution time changes when frequency changes (Example) When f_{cp} or f_{osc} is 270 KHz: $40\mu s \times \frac{250}{270} = 37\mu s$

*Don't care

HEXADECIMAL CODES

The display module data bus accepts 8-bit wide instruction codes which are directed to the instruction register when RS = 0 (low) and R/W = 0 (low). When writing programs, the equivalent hexadecimal code is easier to use than the 8-bit wide instruction codes. Key operational codes are listed below in hexadecimal format.

Command Description	Instruction Code (Hexadecimal Format)	RS Code	R/W Code
Display Control:			
On	0C	0	0
Blank (All memory retained)	0A, 08	0	0
Clear Display & Home Cursor	01	0	0
Home Cursor	02	0	0
Cursor:			
On	0E	0	0
Off	0C	0	0
Wink	0D	0	0
Shift Left	10	0	0
Shift Right	14	0	0
Home	02	0	0
Cursor Travel Upon Character Entry:			
Left	04	0	0
Right	06	0	0
Shift Display with Data Entry:			
Left	07	0	0
Right	05	0	0
Shift Display without Data Entry:			
Left	18	0	0
Right	1C	0	0
Display Data Addresses: (See page 42)			
Home Position 1st Line	80	0	0
Home Position 2nd Line	C0	0	0

INSTRUCTION CODE DEFINITIONS

Outline

Two registers of the HD44780, the Instruction Register (IR) and the Data Register (DR) only can be controlled by MPU directly. Control information is temporarily stored in these registers, prior to internal operation start, to allow interface to various types of MPUs which operate in different speeds from HD44780 internal operation or to allow interface to peripheral control ICs. The HD44780 internal operation is determined by signals sent from the MPU. These signals including register selection signals (RS), read/write signals (R/W) and data bus signals (DB0 ~ DB7) are called instructions in this paragraph. Table on page 38 shows the instructions and the execution time of the instructions. Details are explained in the following sections. The instructions can be divided into the following 4 types:

(1) Instructions that designate the HD44780 functions such as display format, data length, etc.
(2) Instructions that give internal RAM addresses.
(3) Instructions that perform data transfer with internal RAM.
(4) Other instructions.

In the normal use, instructions of category (3), which sends display data, is used most frequently. However, since the HD44780 internal RAM addresses are configured to be automatically incremented (or decremented) by +1 after each data write, MPU program load is lessened. Specifically, display shift is performed concurrently with display data write, and then this enables the user to develop systems with minimum time and maximum efficiency of programming. When an instruction is being executed (during internal operation), the busy flag DB7 is active high. This must be monitored when high speed operation is planned (≈50KHz).

Clear Display

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	0	1

Writes character code "20" (hexadecimal) into all the DD RAM addresses. The cursor returns to Address 0 (A_{DD} = "80") and display, if it has been shifted, returns to the original position. In other words, display disappears and the cursor goes to the left edge of the display (the first line if 2 lines are displayed.)

Return Home

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	1	*

*Don't Care

Returns the cursor to Address 0 (A_{DD} = "80") and display, if it has been shifted, to the original position. The DD RAM contents remain unchanged.

Entry Mode Set

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one upon writing into or reading from the DD RAM a character code. The cursor moves to the right when incremented by one. The same applies to writing and reading of CG RAM.

S: Shifts the entire display to either the right or the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Therefore, the cursor looks as if it stood still with the display only moved. Display is not shifted when reading from the DD RAM. Display is not shifted when S = 0.

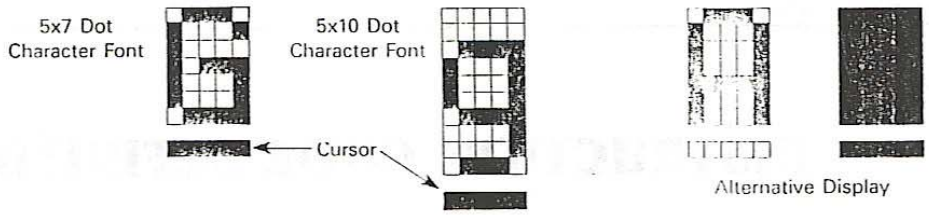
Display ON/OFF Control

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	1	D	C	B

D: Display is turned ON when D = 1 and OFF when D = 0. When display is turned off due to D = 0, the display data remains in the DD RAM and it can be displayed immediately by setting D = 1.

C: The cursor is displayed when C = 1 and not displayed when C = 0. Even if the cursor disappears, function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5x7 dot character font is selected and in the 11th line when 5x10 dot character font is selected.

B: The character residing at the cursor position blinks when B = 1. The blink is done by switching between all the black dots and display characters at 0.4 second interval. The cursor and the blink can be set concurrently.



(a) Cursor Display Example

(b) Blink Display Example

Cursor or Display Shift

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	1	S/C	R/L	*	*

*Don't Care

Shifts the cursor position or display to the right and the left without writing or reading the display data. This function is used for correction or search of display.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Function Set

	RS	R/W	DB7						DB0
Code	0	0	0	0	1	DL	N	F	*	*

*Don't Care

DL: Sets interface data length. Data is sent or received in 8-bit length (DB7 – DB0) when DL = 1 and 4-bit length (DB7 – DB4) when DL = 0. When 4-bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5x7 dots	1/8	—
0	1	1	5x10 dots	1/11	—
1	*	2	5x7 dots	1/16	Cannot display 2 lines with 5x10 dot character font.

*Don't Care

Set CG RAM Address

	RS	R/W	DB7						DB0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits — Lower Order Bits →

Sets the CG RAM address in a binary number of AAAAAA to the address counter, and data is written or read from the MPU related to the CG RAM after this.

Set DD RAM Address

	RS	R/W	DB7							DB0
Code	0	0	1	A_N	A	A	A	A	A	A

← Higher Order Bits — Lower Order Bits →

Sets the DD RAM address in a binary number of A_NAAAAAA to the address counter, and data is written or read from the MPU related to the DD RAM after this. However, when N = 0 (1-line display), A_NAAAAAA is "80" to "CF" (hexadecimal). When N = 1 (2 line display), A_NAAAAAA is '80" to "A7" (hexadecimal) for the first line, and "C0" to "E7" (hexadecimal) for the second line.

Read Busy Flag and Address

	RS	R/W	DB7							DB0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits — Lower Order Bits →

Reads Busy Flag (BF) that indicates the system is internally operating on an instruction received before. When BF = 1, it indicates that internal operation is going on and the next instruction is not accepted until BF is set to "0." Check the BF status before the next write operation and at the same time, the value of the address counter expressed in a binary number of AAAAAA. The address counter is used by both the CG and DD RAM address, and its value is determined by the previous instruction. Address contents are those of the CG RAM or DD RAM previously shown.

Write Data to CG or DD RAM

	RS	R/W	DB7							DB0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits — Lower Order Bits →

Writes binary 8-bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or the DD RAM is to be written is determined by the previous designation (CG RAM address setting or DD RAM address setting). After write, the address is automatically incremented or decremented by one according to entry mode. Display shift also follows the entry mode.

Read Data From CG or DD RAM

	RS	R/W	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Reads binary 8-bit data DDDDDDDD from the CG or the DD RAM. Whether the CG RAM or the DD RAM is to be read is determined by the previous designation. **Prior to inputting this read instruction, either the CG RAM address set instruction or the DD RAM address set instruction must be executed. If it is not done, the first read data becomes invalid, and data of the next address is read normally from the second read.** After read, the address is automatically incremented or decremented by one according to the entry mode. However, display shift is not performed regardless of entry mode types.

DISPLAY DATA ADDRESS CHARTS

(Note: Some charts are different from general instructional data)

1 LINE x 8 CHARACTERS PER LINE
2 LINES x 8 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8
Line 1	80	81	82	83	84	85	86	87
Line 2	C0	C1	C2	C3	C4	C5	C6	C7

SLM 10801 (LINE 1 WITH E)
SLM 20801 (LINE 1 & 2 WITH E)

1 LINE x 16 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF

SLM 11605 / SLM 11606

1 LINE x 16 CHARACTERS PER LINE
2 LINES x 16 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF

SLM 11601 / SLM 11602 / SLM 11603 / SLM 11604 / SLM 11607 } (LINE 1 WITH E)
SLM 21601 / SLM 21602 / SLM 21603 } (LINE 1 & 2 WITH E)

1 LINE x 20 CHARACTERS PER LINE
2 LINES x 20 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3

SLM 12001 / SLM 12002 (LINE 1 WITH E)
SLM 22001 / SLM 22002 (LINE 1 & 2 WITH E)

4 LINES x 16 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
Line 3	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Line 4	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

SLM 41601

1 LINE x 24 CHARACTERS PER LINE
2 LINES x 24 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7

SLM 12401 / SLM 12403 (LINE 1 WITH E)
SLM 22401 / SLM 22402 (LINE 1 & 2 WITH E)

1 LINE x 40 CHARACTERS PER LINE
2 LINES x 40 CHARACTERS PER LINE
4 LINES x 40 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7
Line 3	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 4	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

Note: Address Locations on Lines 1 & 2 are Enabled by E1 Address Locations on Lines 3 & 4 are Enabled by E2

SLM 14001 / SLM 14003 (LINE 1 WITH E)
SLM 24001 / SLM 24002 (LINE 1 & 2 WITH E)
SLM 44001 / SLM 44002 (LINE 1 THRU 4 WITH E1 & E2)

SHELLY associates 14281 Chambers Road • Tustin, California 92680 • (714) 669-9850

1 LINE x 80 CHARACTERS PER LINE

Character

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7

	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
Line 1 (Con't)	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF

SLM 18001

ADDRESS CODES BY QUADRANT (FOR SLM 28001 & SLM 48001)

80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

	Character 1	Character 40 41	80
Line 1	ADDRESS LOCATIONS IN THIS QUADRANT ENABLED BY E1		ADDRESS LOCATIONS IN THIS QUADRANT ENABLED BY E2
Line 2			
Line 3	ADDRESS LOCATIONS IN THIS QUADRANT ENABLED BY E3		ADDRESS LOCATIONS IN THIS QUADRANT ENABLED BY E4
Line 4			

Note: Address codes in all 4 Quadrants are identical. See Quadrant chart above.

SLM 28001 (LINE 1 & 2 WITH E1 & E2)
SLM 48001 (LINE 1 THRU 4 WITH E1, E2, E3 & E4)

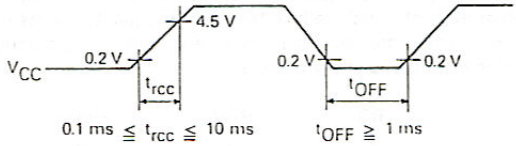
INITIALIZATION OR RESET

Each time power to the module is turned on, an initialization (reset) procedure must be executed. This procedure consists of sending an initial group of instructions to configure the display for normal programming execution. Each module will automatically perform this procedure on power-up (using internal circuitry). However, for this to happen properly, the power supply rise time must meet the parameters shown below. To absolutely insure proper initialization, it might be best to turn the module power on and then send the proper initialization instructions from the microprocessor.

The following instructions are executed by each module automatically on power up:

	Instruction Code	Equiv. Hex Code
(1) Clear display The busy flag is kept in the busy state (BF = 1) until initialization ends. The time is 15ms.	10000000	80 (busy flag)
(2) Function Set .....DL = 1: 8 bits wide interface data N = 0: 1-line display F = 0: 5x7 dot character font	00110000	30 (1st instruction)
(3) Display ON/OFF Control . .D = 0: Display OFF (Blank) C = 0: Cursor OFF B = 0: Blink OFF	00001000	08
(4) Entry Mode Set .....I/O = 1: + 1 (increment) S = 0: No shift	00000110	06
(5) DD RAM is selected		

Because initialization may not be performed completely depending on the rise time of the power supply when it is turned on, pay attention to the adjacent time relationship. t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.



As mentioned above, since some power supplies may not meet the above parameters, it may be better to absolutely ensure proper initialization by sending the following additional initialization instructions from the microprocessor after the above automatic initialization has taken place. These suggested codes create an automatically-incremented, steady line cursor, which is different from the automatic initialization. Also, note that the initial hex code 30, 34 or 38 is sent twice to ensure the module enters the 8-bit data length mode without fail. All initialization is performed with RS and R/W, both 0 (low).

For 8-bit data bus:

1 line, 5x7 character format 30, 30, 06, 0E, 01
1 line, 5x10 character format 34, 34, 06, 0E, 01
2 lines, 5x7 character format only 38, 38, 06, 0E, 01

It is possible to initialize a 2-line module to write to just one line. Using the 30 instruction will improve the contrast ratio by eliminating line 2.

Four-bit data bus microprocessors may also operate the display module. Initialization is crucial and this format must be closely followed. First, we will write the program in hexadecimal code in the same manner as for 8-bit operation, then we will re-write it as actually sent in the 4-bit format. Four-bit operation requires that data be sent twice over the D4 thru D7 bus lines which requires reformatting the 8-bit hexadecimal code for transmission. Memory requirements are also doubled; however, an advantage is the ability to embed all 4 data bits, RS and R/W in a standard 8-bit wide memory. The 8-bit data bus requires at least 9 bits of memory (assuming R/W s l low).

For 4-bit data bus:

1 line, 5x7 character format 20, 20, 06, 0E, 01

Now, the above initialization code must be reformatted as below, to send each hex code twice over the D4 thru D7 bus lines:

22, 00, 22, 00, 00, 66, 00, EE, 00, 1
(Note the single terminating 1. This is crucial.)

1 line, 5x10 character format 24, 24, 06, 0E, 01

Now, reformatted for 4-bit transmission:

22, 44, 22, 44, 00, 66, 00, EE, 00, 1

2 lines, 5x7 character format 28, 28, 06, 0E, 01

Now, reformatted for 4-bit transmission:

22, 88, 22, 88, 00, 66, 00, EE, 00, 1

PROGRAMMING THE CHARACTER GENERATOR RAM (EIGHT USER CREATED CUSTOM CHARACTERS)

The character generator (CG) RAM allows eight custom 5x8 characters or four custom 5x11 characters to be user created and programmed. Once programmed, the newly-created characters or symbols are accessed exactly as if they were in ROM. However, sin e RAM is a volatile memory, power must be continuously maintained. Otherwise, the programming format must be programmed into ..on-volatile external ROM and sent to the display following each display initialization. All dots of the character matrix may be programmed, including the cursor position, if desired.

The module's RAM is divided into two parts: data display and custom character generator (not to be confused with 192-character generator ROM). The CG portion of RAM is located between hex 40 and 7F, and is contiguous. Locations 40 thru 47 hold the first custom CG character, 48 thru 4F the second, 50 thru 57 the third and so forth to 78 thru 7F for the eighth custom CG character. If, during initialization, the display was programmed to automatically increment, then only the single initial address, 40, need be sent. Consecutive row data will automatically appear at 41, 42, etc. until the complete character is formed. All 8 custom CG characters can be programmed in 64 consecutive "writes" after sending the single initial address 40.

CG RAM is 8 bits wide, although only the right-most 5 bits are used for a custom CG character row. The left-most dot of the character row corresponds to D4 in the most significant nibble (XXXD4) of the data bus code with the remaining 4 dots in the row corresponding to the least significant nibble (D3 thru D0), D0 being the right-most dot. Thus, hex 1F equals all dots on and hex 00 equals all dots off. Other examples include hex 15 (HLHLH) equal to 3 dots on and hex 0A (LHLHL) equal to 2 dots on. In each case, the key 5 bits of the 8-bit code, program one row of a custom CG character. When all 7 or 8 rows are programmed, that character is complete. A graphic example is shown below.

RS	R/W	Data	Display	Description
0	0	40		addresses 1st row, 1st CG character
1	0	11	* *	result of 11, 1st row
1	0	0A	* *	result of 0A, 2nd row
1	0	1F	*****	result of 1F, 3rd row
1	0	04	*	result of 04, 4th row
1	0	1F	*****	result of 1F, 5th row
1	0	04	*	result of 04, 6th row
1	0	04	*	result of 04, 7th row
1	0	00		result of 00, 8th row (cursor position)
1	0	15	* * *	1st row, 2nd CG character. Note: addressing not now required, hex 48 is next in the sequence.

CHARACTER FONT DATA CODES

UPPER 4-BIT HEXADECIMAL

LOWER 4-BIT HEXADECIMAL	Lower 4-bit \ Higher 4-bit	0	2	3	4	5	6	7	A	B	C	D	E	F
		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0	xxxx0000	CG RAM (1)												
1	xxxx0001	(2)												
2	xxxx0010	(3)												
3	xxxx0011	(4)												
4	xxxx0100	(5)												
5	xxxx0101	(6)												
6	xxxx0110	(7)												
7	xxxx0111	(8)												
8	xxxx1000	(1)												
9	xxxx1001	(2)												
A	xxxx1010	(3)												
B	xxxx1011	(4)												
C	xxxx1100	(5)												
D	xxxx1101	(6)												
E	xxxx1110	(7)												
F	xxxx1111	(8)												

SOLUTIONS TO INTERFACE PROBLEMS

During the design and development phase of a new product, hardware or software problems between the host processor and the display module sometimes occur. These problems are usually the result of design errors or an improper understanding of the host microprocessor or display module application rules. As an aid to the designer, some typical interface mistakes are shown along with a checklist of possible solutions.

Symptom:

a) Display appears blank: check +5 V and GND at display; check 4, 5, 6 and 7 below.

b) Displayed characters enter unreliably or at random: check 1, 2, 3, and 9 below.

c) Same symptoms as (b) but system has multiple components tied to the data bus: check 8, 9 and 10 below.

d) Descender type characters are "broken". Symptomatic of calling a descender on a two-line display. This cannot be done due to the spacing between lines.

Possible Solution:

1. Transmitting too fast to the display: a) upon initialization allow 15 ms before sending data, b) after transmitting hexidecimal 01 or 02 allow 1.6 ms, c) after all other data allow at least 50 μs.
2. Not generating a positive going enable pulse at least 450 ns wide.
3. All data, RS and R/W signals are not stable for at least 500 ns before, and after, the falling edge of the enable pulse.
4. V_0 pin voltage level improper (see chart for applicable module).
5. Display misconnection: crossed, open or mis-terminated cable.
6. LCD input assumed to be configured as an IC. (This is not so.)
7. Failure to properly initialize the display.
8. Signal levels too low at the display. Insure that 2.4 V (H) appears.
9. Data bus contention. More than one external bus device selected.
10. All data bus components do not have TTL type outputs.

00 01 02 - - - 3F

40 41 42 - - - 7F