Assignment # 4

Due Friday February 8th

Read Chapter 4 Sections 1, 2.2, 2.3, 2.5, and 3. Read also Sections 4.4 to 4.7 that give nice design examples.

1. Chapter 3 Exercise 3.6 (a) and (b).
   Now redo (a) assuming that you can have only 2-stacks AOI gates with no limitations on inputs. (Hint: How do you implement $X + Y$, $X.Y$, or their complements, with a 2-stack, 2-input AOI gate?)
2. Chapter 3 Exercise 3.13. Draw the circuit in DesignWorks, generate the waveforms using the DesignWorks simulator, and hand in your simulation waveform. How to set gate delays will be explained in section. How to set-up the simulation is described in the DesignWorks Help Pages (Generating Useful Output).
3. Chapter 3 Exercise 3.16 (a) and (b).
4. Chapter 4 Exercise 4.11.
5. Chapter 4 Exercise 4.1. Use the minimized logic equation on pg. 224 directly (you don't need to rederive this equation). Use the short-hand notation.
6. Chapter 4 Exercise 4.23 (a), (b) and (c). For part (c) it might be easier to draw a Karnaugh map for $V = 0$ and one for $V = 1$ and then combine prime implicants of the 4 other variables that are common to the 2 K-maps.