# Assignment # 3

## Due Friday February 1st

Read Chapter 3 Sections 1, 3, and 4.

1. (Combinational Logic Design problem)
   Design a logic circuit with 4 inputs $(A, B, C, D)$ and one output $F$ such that $F$ is true $(F = 1)$ when there are pairs of 1's in the first and second input $(A = 1$ and $B = 1)$ or in the third and fourth input $(C = 1$ and $D = 1)$ or all inputs are 1 $(A = 1$ and $B = 1$ and $C = 1$ and $D = 1)$. $F$ is false $(F = 0)$ for all other cases.

   (a) Draw the truth table and Karnaugh map.
   (b) Express both F and F' in minimized sum-of-products form.
   (c) Express both F and F' in minimized product-of-sums form.
   (d) Using your expression for F from (b), draw a circuit (logic) schematic for F using only NAND gates.
   (e) Using your expression for F from (c), draw a circuit (logic) schematic for F using only NOR gates.

2. Chapter 2 Exercise 29

3. (Combinational Logic Design problem)
   Design a Post Office automatic sorter (a very simple one!). Its inputs are:

   - Time of day expressed by 2-bits $A$ and $B$ such that $AB = 00$ during the morning (8 am till noon), $AB = 01$ in the afternoon (noon till 5:00 pm), and $AB = 10$ after hours (5:00 pm till midnight). The sorter does not function between midnight and 8:00 am. The input combination $AB = 11$ is not allowed.
   - Destination of the letter expressed by the input. The variable C is "0" for an East Coast destination and is "1" for a West Coast destination.
   - Speed of delivery. The variable D is "0" for ordinary mail and is "1" for express mail.

   The sorter $S$ places the letter in one of two bins according to the following specifications:

   - In the morning, express letters go to bin 1 $(S = 1)$ and ordinary mail goes to bin 0 $(S = 0)$.
   - In the afternoon, express letters and ordinary mail for the East Coast go to bin 1. Other letters can go in either bin.
   - After hours, East Coast express letters go to bin 1 and ordinary mail for the West Coast goes to bin 0. Other letters can go in either bin.

The assignment is to:

(a) Draw a truth table and a Karnaugh map for the sorter (don't forget to include don't cares).
(b) Write the simplified Boolean expression for $S$.

4. Chapter 3 Exercise 3.2 (a) and 3.3 (c).

5. Create a DesignWorks project for a binary full adder. You can find a block diagram (page 14), a truth table (page 19), and a schematic diagram (page 250) in the textbook. Perform the following (it should be wise to do steps (a) and (b) in the same session).

   (a) Draw the full adder schematics in DesignWorks using standard logic gates from the *PrimGate* library. Label input $A$, $B$ and $Cin$ and outputs $Sum$ and $Cout$. Use "PortIn" and "PortOut" symbols from the *Pseudo* library to label inputs and outputs. Turn in your schematic drawing.
   (b) Create your own full adder part (cf. page 14 for what it should like and see the "Create your own parts" help page for the DesignWorks process). Label it "FullAdder" and save it in your private library. Attach binary probes from the *Primio* library to $Sum$ and $Cout$. Attach a "hex keyboard" from the *Primio* library to $A$, $B$ and $Cin$ (Note: the bottom wire on the hex keyboard is the LSB). Select digits from the keyboard and verify that your outputs are correct. Turn in your schematic drawing with the keyboard and probes.
   (c) Cascade four full-adders (four of your blocks from part (b)) as in Figure 5.6 page 249. Label the inputs $A0, A1, A2, A3, B0, B1, B2, B3$; Label the outputs $S0, S1, S2, S3$ and $C4$. Attach five binary probes from the *Primio* library to the four $S$ digits and $C4$. Connect $Cin$ for the first adder to logic 0. Attach two "hex keyboard" from the *Primio* library to your $A$ and $B$ inputs. Verify that your adder computes the sums $A + B$ correctly, where
      i. $A = 0$ and $B = 3$
      ii. $A = 7$ and $B = 7$
      iii. $A = 9$ and $B = 7$

      Turn in three schematic sheets, showing the correct output for these three cases on the binary probes.