

CSE370: Introduction to Digital Design
Winter 2000

Homework Set 7 – Part A

DUE: WEDNESDAY March 1, 2000, 12:30 pm

Please show *all* of your work. In certain problems, you may be asked to use Design Works. Otherwise, solutions do not have to be typeset, but may be if desired. In any case, your solutions must be legible. Please staple all the pages together. Make it clear which problem is which (especially important for the printouts from Design Works).

- 1) Read the handout on Verilog (from Mano and Kime). Then answer these questions based on it:
 - A. There is a discrepancy between Figure 3-14 and the Verilog which supposedly corresponds to in Figure 3-44. Find the discrepancy and correct the Verilog (do not change the schematic).
 - B. Comparing the ripple-carry adder in Fig. 3-28 to its Verilog module “adder_4_v” in Fig. 3-50: there are some parts and/or wires in the Verilog that either don’t appear in the schematic or are named differently. Carefully label the schematic to show all of the names used within adder_4_v. (You don’t have to use names internal to subparts, such as names inside full_adder_v, etc.).
 - C. The “conditional operator” used in Fig. 3-48 and elsewhere looks pretty weird. Is there anything like it in any programming language you know??
 - D. The Verilog in Fig. 4-34 for the sequence recognizer has three separate “always” blocks. Would it be possible to combine any or all of those blocks, and get the same behavior? If your answer is yes, show how it would be done. If your answer is no, explain why not.