University of Washington – Computer Science & Engineering

Spring 2020 Instructor: Clarice Larson 2020-05-19

CSE 369 QUIZ 2

Name: _____

UWNetID: _____

Please do not turn the page until 11:30.

Instructions

- This quiz contains 4 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is open book and open notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- You have 25 minutes to complete this quiz.

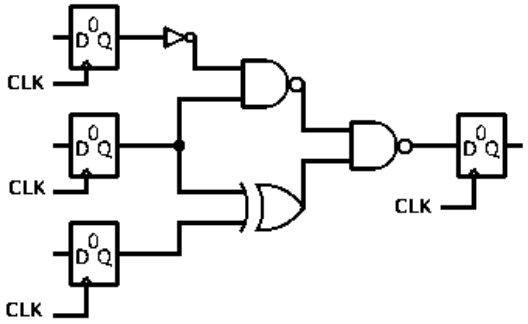
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) SL & Timing	6	
(2) FSM Implementation	10	
(3) FSM Design	10	
Total:	**26**	

Question 1: Sequential Logic & Timing [6 pts]

Consider the following circuit with $t_{\text{XOR}} = \mathbf{20\ ns}$ (10^{-9} s), $t_{\text{NAND}} = \mathbf{10\ ns}$ (10^{-9} s), $t_{\text{NOT}} = \mathbf{5\ ns}$, $t_{\text{setup}} = \mathbf{5\ ns}$, and $t_{\text{C2Q}} = \mathbf{30\ ns}$.



(A) Calculate the **minimum clock period** that will allow the circuit to function correctly. Make sure to *include units*. [3 pts]

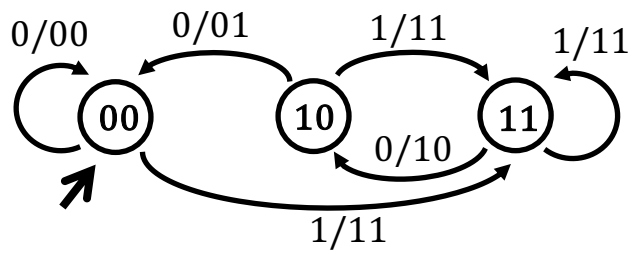
$t_{\text{period}} \geq$

(B) Calculate the **maximum hold time** that will allow the circuit to function correctly. Make sure to *include units*. [3 pts]

$t_{\text{hold}} \leq$

Question 2: Finite State Machine Implementation [10 pts]

(A) Fill in the provided truth table based on the FSM shown. [2 pts]



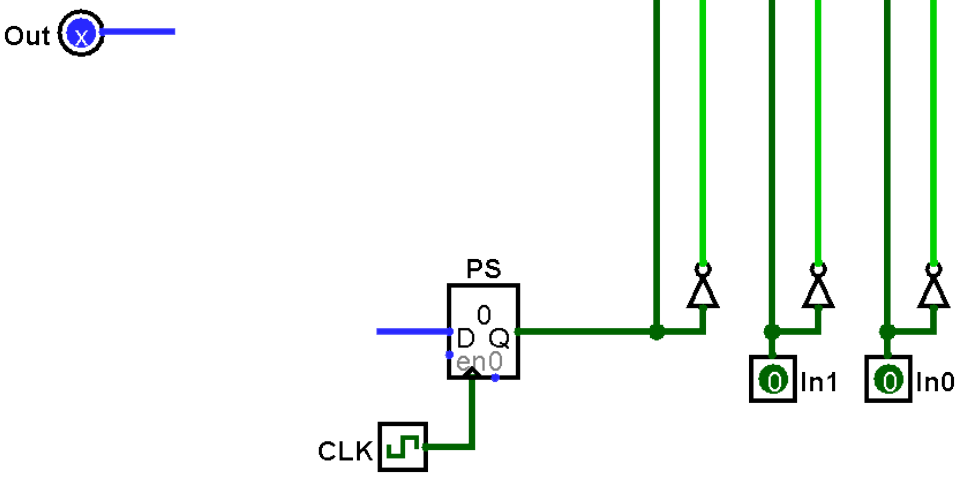
PS_1	PS_0	In	NS_1	NS_0	Out_1	Out_0
0	0	0	0	0	0	0
0	0	1			1	1
0	1	0	X	X	X	X
0	1	1	X	X		
1	0	0			0	1
1	0	1	1	1	1	1
1	1	0	1	0		
1	1	1	1	1	1	1

(B) Complete the circuit diagram below using *minimal logic* based on the truth table shown below. You are welcome to use 2- and 3-input logic gates. [8 pts]

PS	In_1	In_0	NS	Out
0	0	0	0	X
0	0	1	X	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	X
1	0	1	1	0
1	1	0	X	0
1	1	1	0	0

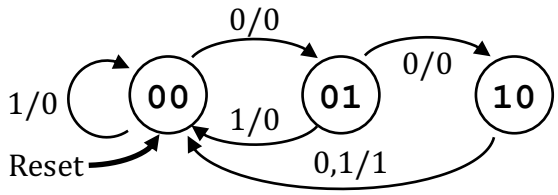
Wire connection:

Wire crossing:



Question 3: Finite State Machine Design [10 pts]

For this problem, consider the FSM below:



(A) Answer the following about the corresponding *truth table*. [2 pts]

Rows:	Rows of Don't Cares:

(B) Complete the testbench `initial` block to *thoroughly* test the state diagram. Even though they may be unnecessary, please fill in all blanks. You are welcome to fill out the Verilog comments to help you keep track of state, but these will not be graded. [6 pts]

```
initial begin
                        In <= 1;        // state: 00
   @(posedge clk);      In <= _____;    // state: _____
   @(posedge clk);      In <= 1;        // state: _____
   @(posedge clk);      In <= _____;    // state: _____
   @(posedge clk);      In <= _____;    // state: _____
   @(posedge clk);      In <= 0;        // state: _____
   @(posedge clk);      In <= _____;    // state: _____
   @(posedge clk);      In <= _____;    // state: _____
   @(posedge clk);      In <= _____;    // state: _____
   @(posedge clk);                      // state: _____
   $stop();
end
```

(C) What two 3-input sequences does this FSM "recognize" (*i.e.* when it outputs a `1`)? [2 pt]
