University of Washington – Computer Science & Engineering

Autumn 2016 Instructor: Justin Hsia 2016-11-22

CSE 369 QUIZ 2

Name: _Perry_Perfect_____

UWNetID: _1234567_____

Please do not turn the page until 10:30.

Instructions

- This quiz contains 4 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

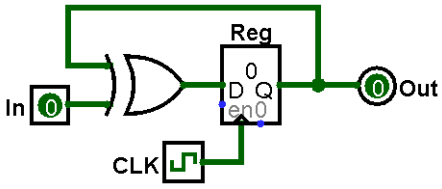
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) SL & Timing	8	8
(2) FSM Implementation	10	10
(3) FSM Design	9	9
Total:	**27**	**27**

Question 1: Sequential Logic & Timing [8 pts]

Consider the following circuit diagram with a clock period of **500 ps** (10^{-12} s), setup time of **80 ps**, hold time of **50 ps**, and clock-to-q delay of **100 ps**. Fill in your answers in the boxes below.



(A) If the input `In` changes exactly on clock triggers, what are the limits on the XOR gate delay that ensure proper behavior? Write "**n/a**" if no such limit exists. ***Include units!*** [4 pts]

Max t_{XOR} = 320 ps	Min t_{XOR} = 50 ps

Critical path is from register and through XOR, so $t_{C2Q} + t_{XOR} \leq t_{period} - t_{setup}$.
$t_{XOR,max} = 500 - 80 - 100 = 320$ ps.
Shortest path is from input and through XOR, so $t_{in} + t_{XOR} \geq t_{hold}$.
$t_{XOR,min} = 50 - 0 = 50$ ps.

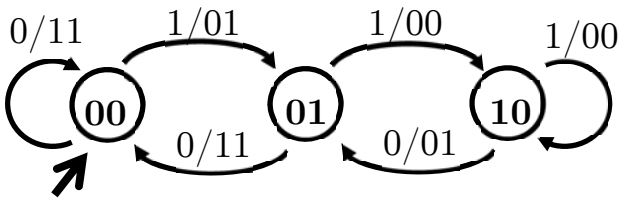
(B) We choose a gate with t_{XOR} = **100 ps** and complicate the input logic so that the input `In` changes t_{in} after each clock trigger. Within each clock cycle (between 0 and 500 ps) for what ranges of t_{in} will we get proper behavior? Answer using interval notation: $[t_{start}, t_{end}]$. [4 pts]

[0 , 320] ps and [450 , 500] ps

The unsafe region is from t_{setup} before a clock trigger to t_{hold} after a clock trigger, which is roughly [420, 550] ps. Accounting for t_{XOR}, then the unsafe region is [320, 450] ps.

Question 2: Finite State Machine Implementation [10 pts]

(A) Fill in the provided truth table based on the FSM shown. [2 pts]



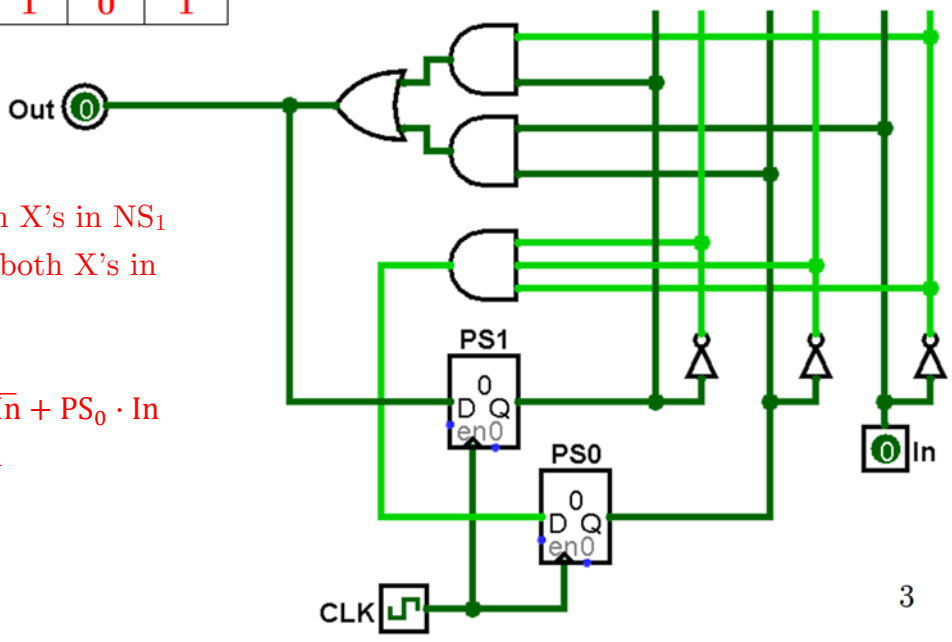
PS_1	PS_0	In	NS_1	NS_0	Out_1	Out_0
0	0	0	0	0	1	1
0	0	1	0	1	0	1
0	1	0	0	0	1	1
0	1	1	1	0	0	0
1	0	0	0	1	0	1
1	0	1	1	0	0	0
1	1	0	X	X	X	X
1	1	1	X	X	X	X

(B) Complete the circuit diagram below using *minimal logic* based on the truth table shown below. You are welcome to use 2- and 3-input logic gates. [8 pts]

PS_1	PS_0	In	NS_1	NS_0	Out
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	1	0	1
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	**1**	**0**	**1**
1	1	1	**1**	**0**	**1**

Wire connection:

Wire crossing:



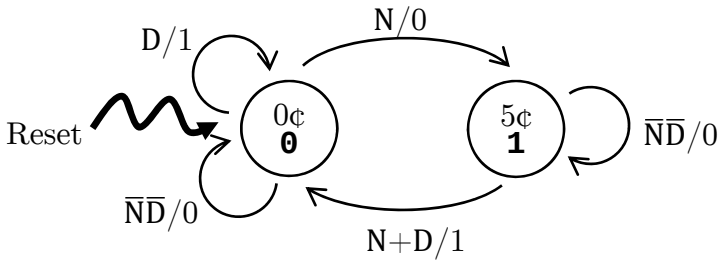
In K-maps, use both X's in NS_1 and Out as 1's and both X's in NS_0 as 0's.

$NS_1 = Out = PS_1 \cdot \overline{In} + PS_0 \cdot In$

$NS_0 = \overline{PS_1} \cdot \overline{PS_0} \cdot \overline{In}$

Question 3: Finite State Machine Design [9 pts]

Recall the 10¢ gumball-dispensing, no-change-giving vending machine FSM from lecture:



(A) Complete the testbench `initial` block to ***thoroughly*** test the FSM. Even though they may be unnecessary, please fill in all blanks. Don't worry about situations we don't expect to see during normal operation. [4 pts]

```
initial begin
                        N <= 0;     D <= 0;
     @(posedge clk);    N <= 1;     D <= 0;
     @(posedge clk);    N <= 1;     D <= 0;

     @(posedge clk);    N <= _0_;   D <= _1_;

     @(posedge clk);    N <= _1_;   D <= _0_;

     @(posedge clk);    N <= _0_;   D <= _0_;

     @(posedge clk);    N <= _0_;   D <= _1_;
     @(posedge clk);
     $stop();
end
```

Could also have the first line as the last.

(B) Due to inflation, we decided to make the gumballs 25¢, how many states and state bits would we need? [2 pts]

States for 0¢, 5¢, 10¢, 15¢, 20¢

States: 5	State bits: 3

(C) If we kept the cost of gumballs at 10¢ but got greedy and also accepted quarters (25¢), draw the new state diagram below. *Use as few arrows as possible.* [3 pts]