University of Washington – Computer Science & Engineering

Winter 2023 Instructor: Chris Thachuk 2023-01-31

CSE 369 QUIZ 1

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Please do not turn the page until 12:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 (+5) minutes to complete this quiz.

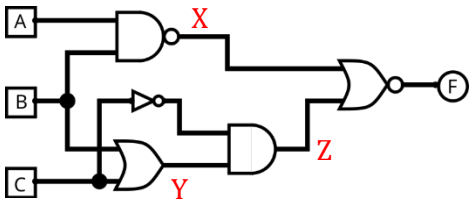
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	10	10
Total:	**23**	**23**

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]



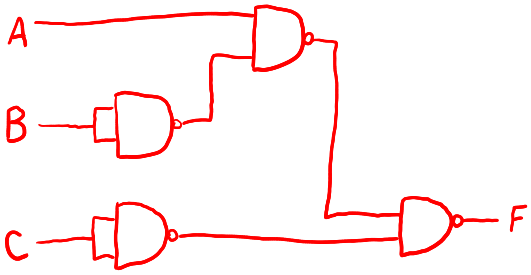
$\mathbf{F} = \overline{(\overline{A} \cdot \overline{B}) + (\overline{C} \cdot (B + C))}$

$X = \overline{A \cdot B}$ [0.5 pt]
$Y = B + C$ [0.5 pt]
$Z = \overline{C} \cdot Y$ [0.5 pt]
$F = \overline{X + Z}$ [0.5 pt]

(B) Find a minimal implementation of the function below using only **2-input NAND gates**. *We will only accept circuit diagrams.* [6 pts]

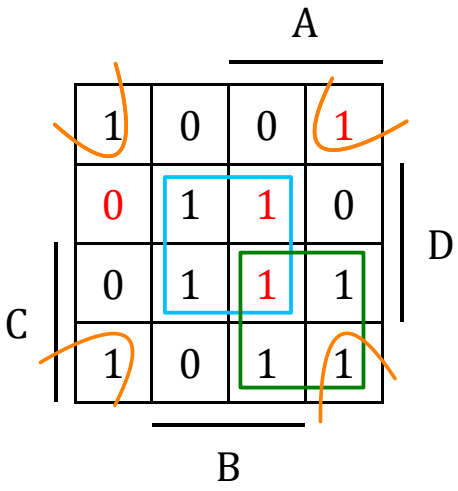
$$F = \overline{(\overline{A} + B)\overline{C}}$$

[2 pt] Valid gate conversion from expression
[2 pt] DeMorgan's applications (in expression or gates)
[2 pt] Conversion of extra NOTs to NANDs



Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

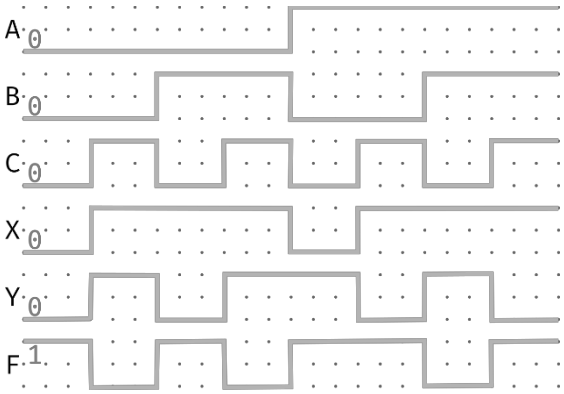


$= BD + AC + \overline{B}\,\overline{D}$

[2 pt] X choices
[1pt each] Correct term / grouping
[-0.5pt each] Smaller grouping used
[-0.5pt each] Extra grouping included

Question 3: Waveforms & Verilog [10 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pts]




```
module Mystery (F, A, B, C);
   output logic F;
   input  logic A, B, C;
   logic        X, Y;

   or  G1 (X, B, C);

     // or assign X = B | C;

   xor G2 (Y, A, C);

     // or assign Y = A ^ C;

   nand G3 (F, X, Y);
endmodule
```

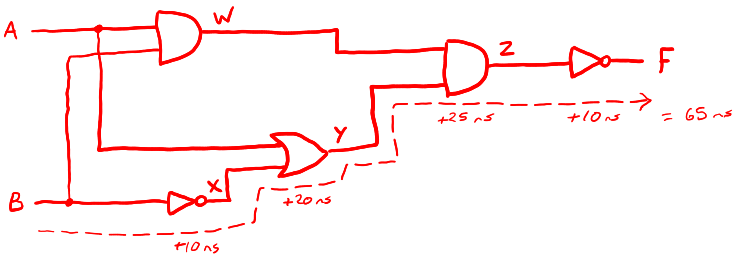
For both X and Y:
[2 pt] Correct input signals
[1pt] Correct gate uses
Overall:
[1 pt] Correct Verilog syntax

(B) For the Verilog module `FastOrSlow`, assume the logic delays shown. If the values of A and B first become known at $t = 0$ and output F is unknown at $t = 0$, at what time is F first guaranteed to become known? *Remember to include units. The correct time is all that is required, but an incorrect answer can receive partial credit for correctly drawing the circuit diagram.* [3 pt]

NOT	AND	OR
10 ns	25 ns	20 ns

```
module FastOrSlow (F, A, B);
   output logic F;
   input  logic A, B;
   logic        W, X, Y, Z;

   and    G1 (W, A, B);
   not    G2 (X, B);
   or     G3 (Y, A, X);
   and    G4 (Z, W, Y);
   not    G5 (F, Z);
endmodule
```



t = 65 ns