

# CSE 369 QUIZ 1

Name: \_\_\_\_\_  
Student ID  
Number: \_\_\_\_\_

Please do not turn the page until 12:30.

## Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 (+5) minutes to complete this quiz.

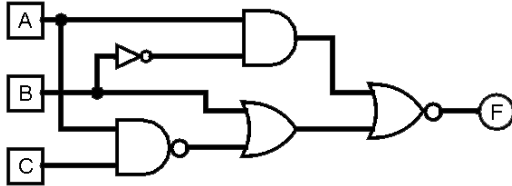
## Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	
(2) K-map	5	
(3) Waveforms & Verilog	12	
Total:	25	

Question 1: Combinational Logic Gates [8 pts]

- (A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and  $\bar{\phantom{x}}$  (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]



- (B) Find a minimal implementation of the function below using only 2-input NOR gates. *We will only accept circuit diagrams.* [6 pts]

$$F = \overline{AB} + C\overline{D}$$

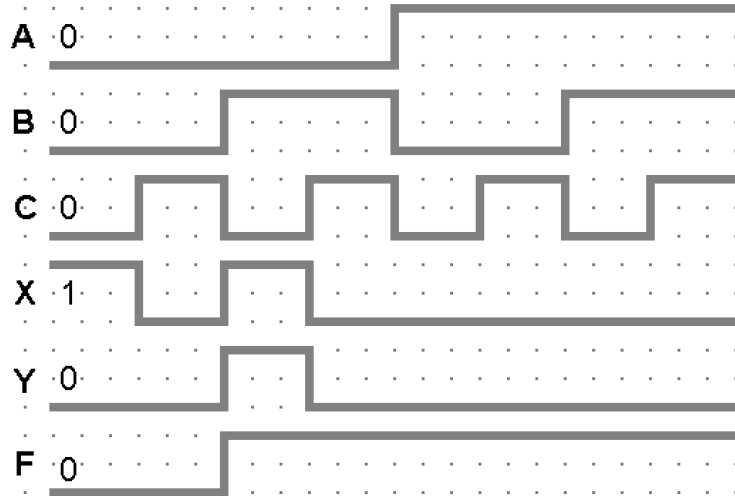
Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

		A				
		X	0	0	1	
		0	X	0	0	
		1	0	X	1	D
C		1	0	1	X	
		B				

Question 3: Waveforms & Verilog [12 pts]

- (A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pts]



```

module Mystery (F, A, B, C);
    output logic F;
    input logic A, B, C;
    logic      X, Y;

    _____;
    _____;

    xnor    G3 (F, X, Y);
endmodule

```

- (B) We only have the 2-input logic gates at right available to us. Given the logic delays shown, draw out the circuit diagram of the *fastest* implementation of the Verilog statement below. [5 pts]

XOR	NAND	OR
6 ns	7 ns	10 ns

Hint: Build a truth table first.

```

assign F = B ^ (~A | B);

```