University of Washington – Computer Science & Engineering

Winter 2020 Instructor: Justin Hsia 2020-02-04

CSE 369 QUIZ 1

Name: _____

Student ID Number: _____

Please do not turn the page until 11:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

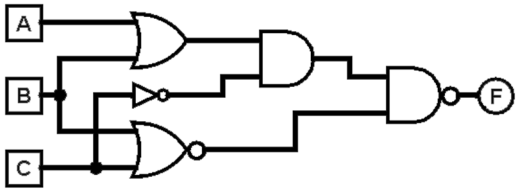
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	
(2) K-map	5	
(3) Waveforms & Verilog	11	
Total:	**24**	

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]



(B) Find a minimal implementation of the function below using only **2-input NOR gates**. *We will only accept circuit diagrams.* [6 pts]

$$F = \overline{(\mathrm{A} + \mathrm{B})\overline{\overline{\mathrm{C}}\mathrm{D}}}$$

Question 2: Karnaugh Maps [5 pts]

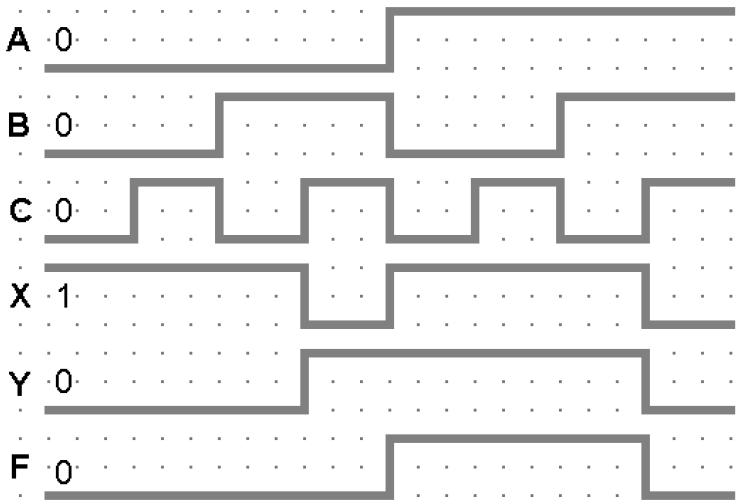
Find the *minimum sum-of-products solution* for the K-map shown below.

C \ AB	00	01	11	10
00	X	0	0	0
01	1	1	1	X
11	X	1	0	1
10	0	0	0	X

D

Question 3: Waveforms & Verilog [11 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pt]




```
module Mystery (F, A, B, C);
      output F;
      input  A, B, C;
      wire   X, Y;

      ____________________________________

      ____________________________________
      and    G3 (F, X, Y);
endmodule
```

(B) The snippet below is from a Verilog testbench. Draw out the waveforms. [4 pts]

```
logic [1:0] S;
initial begin
  S = 2'b00; #30; S[1] = 1; #10; S = S | 2'b01; #40;
  S = {S[0] ^ S[1], S[0] & S[1]}; #40;
end
```