

# CSE 369 QUIZ 1

Name: \_\_\_\_\_

UWNetID: \_\_\_\_\_

**Please do not turn the page until 10:30.**

## Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

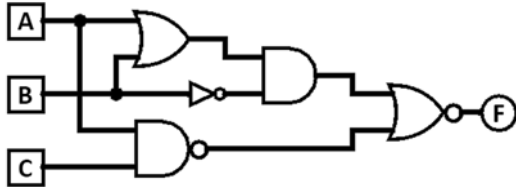
## Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

| Question                | Points    | Score |
|-------------------------|-----------|-------|
| (1) CL Gates            | 8         |       |
| (2) K-map               | 5         |       |
| (3) Waveforms & Verilog | 11        |       |
| <b>Total:</b>           | <b>24</b> |       |

**Question 1: Combinational Logic Gates [8 pts]**

- (A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and  $\bar{\phantom{x}}$  (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]



- (B) Find a minimal implementation of the function below using only **2-input NAND gates**. *We will only accept circuit diagrams.* [6 pts]

$$F = \bar{A} + B + CD$$

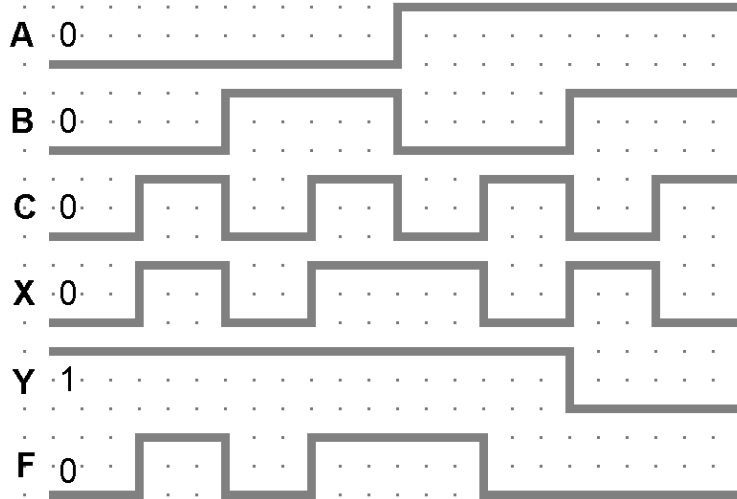
**Question 2: Karnaugh Maps [5 pts]**

Find the *minimum sum-of-products solution* for the K-map shown below.

|   |   |   |   |   |   |
|---|---|---|---|---|---|
|   |   | A |   |   |   |
|   |   | 0 | 1 | X | X |
| C | 1 | 1 | 1 | 1 | X |
|   | 0 | 0 | 0 | 0 | 1 |
|   | 0 | 0 | X | 1 | 0 |
|   |   |   |   |   |   |
|   |   | B |   |   |   |
|   |   | D |   |   |   |

**Question 3: Waveforms & Verilog [11 pts]**

- (A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pt]



```

module Mystery (F, A, B, C);
    output F;
    input A, B, C;
    wire X, Y;

    _____
    _____

    and G3 (F, X, Y);
endmodule
    
```

- (B) Our DE1-SoC is broken and we only have the 1- or 2-input logic gates shown at right available to us. Given the logic delays shown, draw out the circuit diagram of the *fastest* implementation of the Verilog statement below. [4 pts]

| NOT  | OR    | NOR   |
|------|-------|-------|
| 5 ns | 30 ns | 20 ns |

Hint: How many inputs are there? How many gates do you think you'll need?

```

assign F = ~((~A | B) & ~B);
    
```