University of Washington – Computer Science & Engineering

Spring 2024 Instructor: Justin Hsia 2024-04-23

CSE 369 QUIZ 1

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Please do not turn the page until 2:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 (+5) minutes to complete this quiz.

Advice

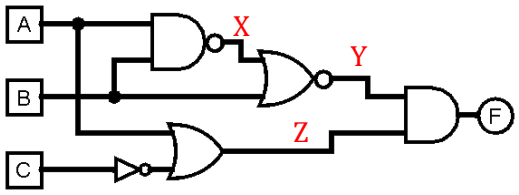
- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	13	13
Total:	**26**	**26**

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]

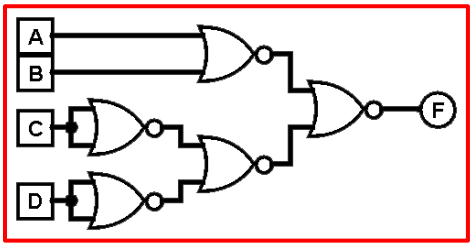
$\mathbf{F = (\overline{A \cdot B} + B) \cdot (A + \bar{C})}$



$X = \overline{A \cdot B}$ [0.5 pt]
$Y = \overline{X + B}$ [0.5 pt]
$Z = A + \bar{C}$ [0.5 pt]
$F = Y \cdot Z$ [0.5 pt]

(B) Find a minimal implementation of the function below using only **2-input NOR gates**. *We will only accept circuit diagrams.* [6 pts]

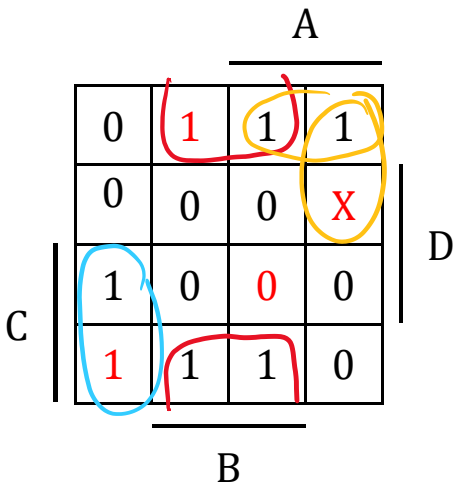
$$F = (A + B)(\overline{CD})$$



[2 pt] Valid gate conversion from expression
[2 pt] DeMorgan's applications (either in expression or gates)
[2 pt] Conversion of extra NOTs to NORs

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

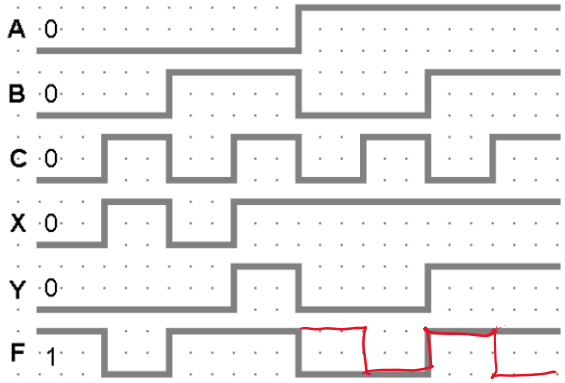


$= B\bar{D} + \bar{A}\bar{B}C + A\bar{C}\bar{D}$
or $+ A\bar{B}\bar{C}$

[2 pt] X choices
[1 pt each] correct term/grouping
[-0.5 pt each] smaller grouping used
[-0.5 pt each] extra grouping included

Question 3: Waveforms & Verilog [13 pts]

(A) Consider the Verilog simulated test bench waveforms shown. Assume all delays are set to 0. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pts]




```
module Mystery (F, A, B, C);
   output logic F;
   input  logic A, B, C;
   logic        X, Y;

   or  G1 (X, A, C);
   // or assign X = A | C;

   and G2 (Y, B, X);
   // or assign Y = B & X;

   xnor   G3 (F, X, Y);
endmodule
```

The following table will be used for both Part B and Part C:

A	B	C	F	Match?	Tested?
0	0	0	1	Y	Y
0	0	1	0	Y	Y
0	1	0	1	Y	Y
0	1	1	1	Y	N
1	0	0	1	N	Y
1	0	1	0	Y	Y
1	1	0	1	Y	Y
1	1	1	0	N	Y

(B) The `F` column shows the intended/desired functionality of the signal `F`. Complete the `Match?` column with **Y/N** to identify whether the waveform above matches the desired functionality. [2 pts]

(C) A test bench for the `Mystery` module (with inputs `A`, `B`, `C`) is shown on the right. Complete the `Tested?` column with **Y/N** to verify which combinations are currently being tested. [4 pts]

```
module Mystery_tb ();
   logic F, A, B, C;

   initial begin
                              #10;
      A = 1; B = 1; C = 1;    #10;
                     C = 0;   #10;
            B = 0;   C = 1;   #10;
      A = 1;                  #10;
                     C = 0;   #10;
      A = 0;         C = 1;   #10;
                     C = 0;   #10;
            B = 1;            #10;
   end
endmodule
```