University of Washington – Computer Science & Engineering

Spring 2022 Instructor: Mark Wyse 2022-04-26

CSE 369 QUIZ 1

Name: _____

Student ID Number: _____

Please do not turn the page until 12:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 (+5) minutes to complete this quiz.

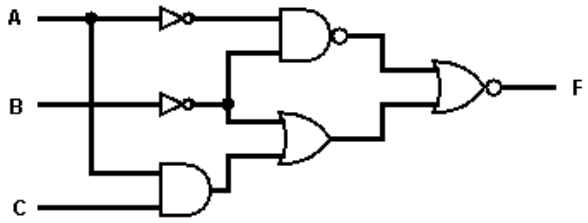
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	
(2) K-map	5	
(3) Waveforms & Verilog	12	
Total:	**25**	

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]



(B) Find a minimal implementation of the function below using only **2-input NAND gates**. *We will only accept circuit diagrams.* [6 pts]

$$F = \overline{\overline{\mathrm{B}}C + \overline{\mathrm{A}}D}$$

Question 2: Karnaugh Maps [5 pts]

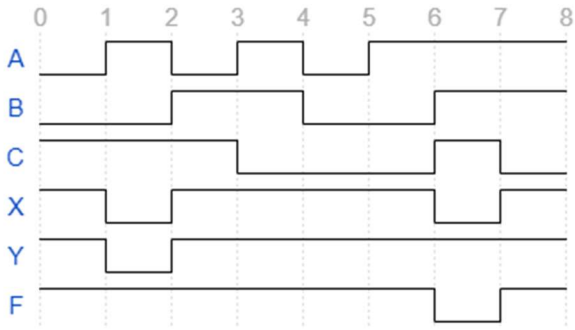
Find the *minimum sum-of-products solution* for the K-map shown below.

C \ AB	00	01	11	10
00	1	1	0	X
01	X	X	X	0
11	0	1	0	0
10	1	0	0	1

D

Question 3: Waveforms & Verilog [12 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [6 pts]




```
module Mystery (
  output logic F
  ,input logic A, B, C
  );
  logic X, Y;

  ____________________________________________________________________;

  ____________________________________________________________________;

  xnor G3 (F, X, Y);
endmodule
```

(B) Complete the implementation of a 2:1 Multiplexer in the module definition given below, using structural Verilog. [2 pts]

```
module mux2_1 (output logic out, input logic a, b, sel);

  ____________________________________________________________________;
endmodule
```

(C) What is the width of the signal **bus** in the Verilog statement: **`logic [N-2:0] bus;`** [1 pts]

(D) Write a Verilog statement that replicates the least significant 3 bits of the **bus** signal above twice and pads the result with zeros to create a **10-bit** signal, which is assigned to **F** below. [2 pts]

```
assign F = ____________________________________________________________;
```

(E) Verilog uses 4-state values for variables. What does the **X** state represent? [1 pts]