CSE 369 QUIZ 1

Name: _Molly_Model_____

UWNetID: _model_____

Please do not turn the page until 11:40.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is open book and open notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
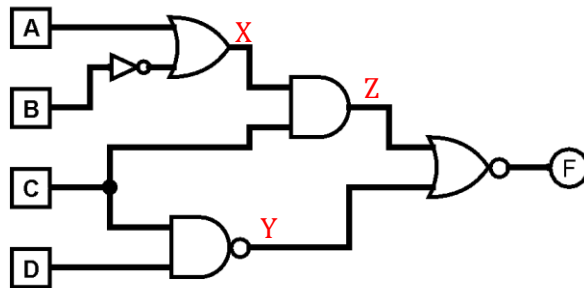- You have 20 minutes to complete this quiz.

Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	11	11
Total:	24	24

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.*
Remember to use + (OR), · (AND), and ‾ (NOT) as well as any necessary parentheses to
make your answer unambiguous. [2 pts] $F = \overline{((A + \overline{B}) \cdot C) + (\overline{C \cdot D})}$

$X = A + \overline{B}$ [0.5 pt]
$Y = \overline{C \cdot D}$ [0.5 pt]
$Z = X \cdot C$ [0.5 pt]
$F = \overline{Y + Z}$ [0.5 pt]

(B) Find a minimal implementation of the function below using only **2-input NOR gates**. *We will only accept circuit diagrams.* [6 pts]

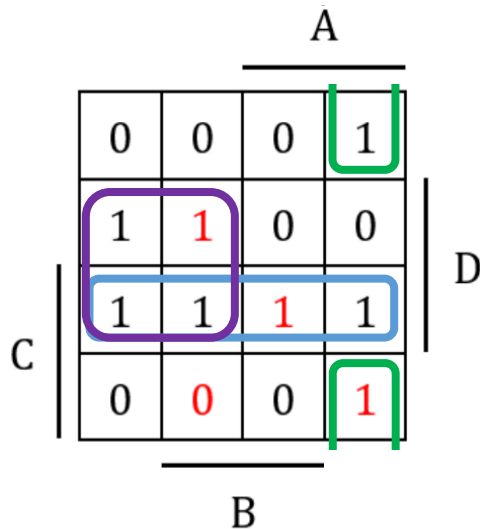$$F = \left(\overline{A \cdot \overline{B}} \right) \cdot (C + D)$$
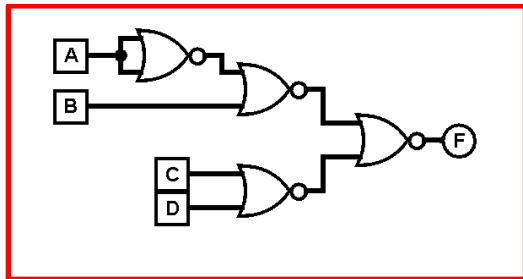
[3 pt] Valid gate conversion from expression
[2 pt] DeMorgan's applications (either in expression or gates)
[1 pt] Conversion of extra NOTs to NANDs

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

$F = CD + \overline{A}D + A\overline{B}\,\overline{D}$

[2 pt] X choices
[1 pt each] correct term/grouping
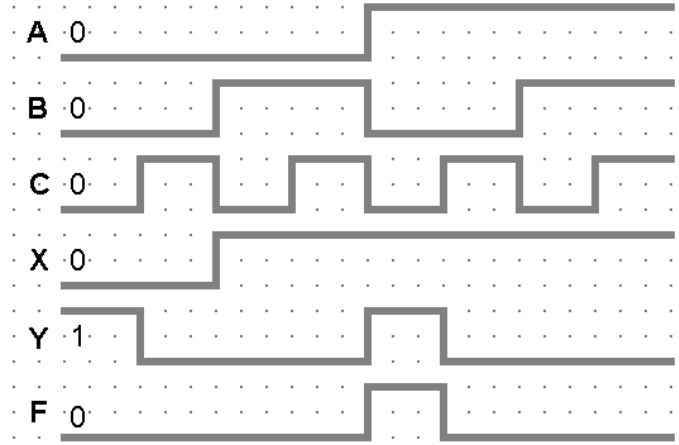[-0.5 pt each] smaller grouping used
[-0.5 pt each] extra grouping included

Question 3: Waveforms & Verilog [11 pts]

(A)   Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [8 pts]

For both X and Y:
[2 pt] Correct input signals
[1 pt] Correct gate used
[1 pt] Correct Verilog syntax


```
module Mystery (F, A, B, C);
      output logic F;
      input  logic A, B, C;
      logic   X, Y;

      or G1 (X, A, B); or assign X = A | B;

      nor G2 (Y, B, C); or assign Y = ~(B | C);

      and G3 (F, X, Y);
endmodule
```
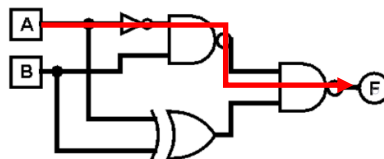
(B)   Given the Verilog module `Circuit` below, assume the logic delays shown. If the values of inputs A and B first become known at $t = 0$ and output F is unknown at $t = 0$, at what time will you know the value of F? [3 pts]

XOR	NAND	NOT
10 ns	8 ns	4 ns

```
module Circuit (F, A, B);
      output logic F;
      input  logic A, B;

      assign F = ~(~(~A & B) & (A ^ B));
endmodule
```


$t = 20$ ns