University of Washington – Computer Science & Engineering

Spring 2017 Instructor: Justin Hsia 2017-04-25

CSE 369 QUIZ 1

Name: _____

UWNetID: _____

Please do not turn the page until 10:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

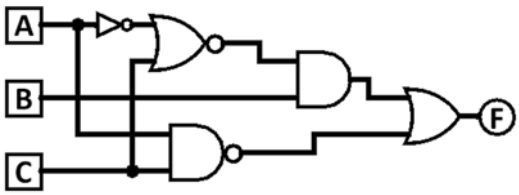
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	
(2) K-map	5	
(3) Waveforms & Verilog	11	
Total:	**24**	

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and $^{-}$ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]



(B) Find a minimal implementation of the function below using only **2-input NOR gates**. *We will only accept circuit diagrams.* [6 pts]

$$F = \overline{\overline{A\bar{B}} + \bar{C}\bar{D}}$$

Question 2: Karnaugh Maps [5 pts]

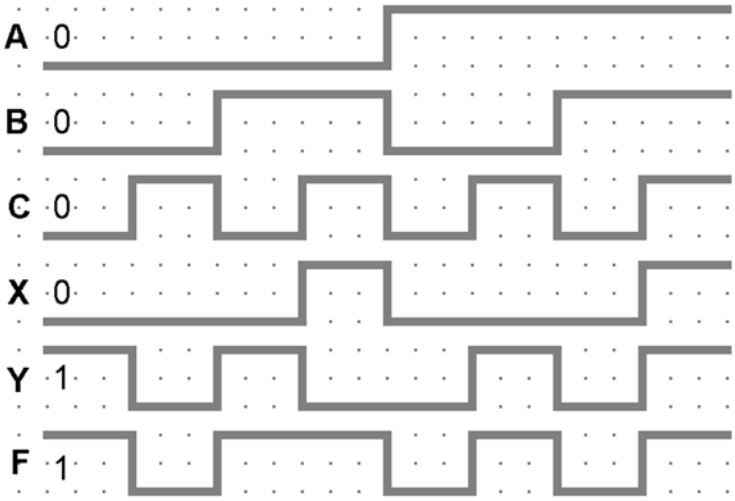
Find the *minimum sum-of-products solution* for the K-map shown below.

C \ AB	00	01	11	10
00	0	0	0	1
01	1	X	0	X
11	X	0	0	1
10	0	0	1	X

D

Question 3: Waveforms & Verilog [11 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [8 pt]




```
module Mystery (F, A, B, C);
     output F;
     input  A, B, C;
     wire   X, Y;

     _____________________________________

     _____________________________________

     or G3 (F, X, Y);
endmodule
```

(B) For the Verilog module `Circuit` below, assume an implementation of *only* NOT, AND, and OR gates that each have a delay of 20 ns. If the values of inputs A and B first become known at $t = 0$ and output F is unknown at $t = 0$, at what time is F first *guaranteed* to become known? *Remember to include units.* [3 pts]

```
module Circuit (F, A, B);
     output F;
     input  A, B;

     assign F = ~((~A | B) & ~B);

endmodule
```

$t =$