University of Washington – Computer Science & Engineering

Autumn 2016 Instructor: Justin Hsia 2016-11-01

CSE 369 QUIZ 1

Name: _____

UWNetID: _____

Please do not turn the page until 10:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

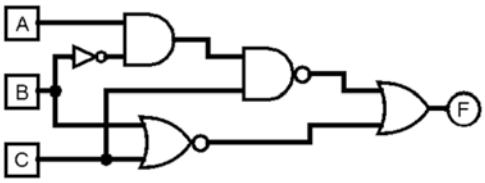
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	
(2) K-map	5	
(3) Waveforms & Verilog	11	
Total:	**24**	

Question 1: Combinational Logic Gates [8 pts]

(A) Write out a Boolean expression for the circuit diagram below. No need to simplify. [2 pts]



(B) Find a minimal implementation of the function below using only **2-input NOR gates**. [6 pts]

$$F = \overline{\bar{A}\bar{B}(C + D)}$$

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

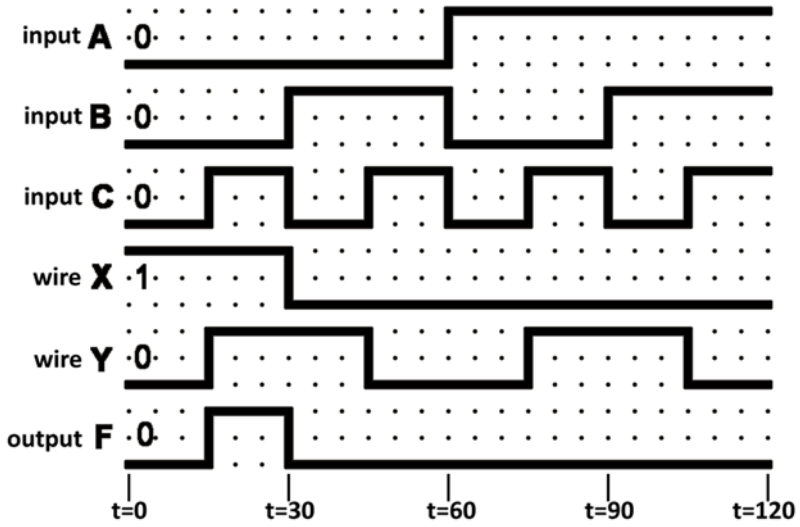
C \ AB	00	01	11	10
00	0	0	0	X
01	1	1	X	1
11	1	X	1	0
10	X	0	0	0

D

Question 3: Waveforms & Verilog [11 pts]

For both parts below, consider the following desired truth table and the Verilog simulated testbench waveforms shown below.

A	B	C	F
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**0**
1	0	0	**0**
1	0	1	**1**
1	1	0	**0**
1	1	1	**1**



(A) Identify the time interval(s) where the testbench output does not match the desired functionality. Each horizontal tick represents 5 time units. [3 pts]

(B) If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below based on the testbench output. [8 pts]

```
module Mystery (F, A, B, C);
    output F;
    input  A, B, C;
    wire   X, Y;

    _____________________________________

    _____________________________________

    and G3 (F, X, Y);
endmodule
```