University of Washington – Computer Science & Engineering

Autumn 2016   Instructor: Justin Hsia   2016-11-01

CSE 369 QUIZ 1

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Please do not turn the page until 10:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	11	11
Total:	24	24

Question 1: Combinational Logic Gates [8 pts]

(A)   Write out a Boolean expression for the circuit diagram below. No need to simplify. [2 pts] $\mathbf{F = \overline{A\overline{B}C} + \overline{B + C}}$
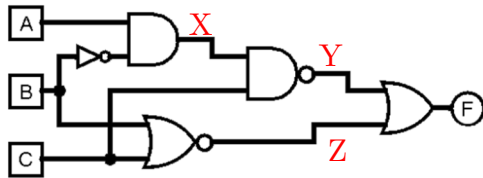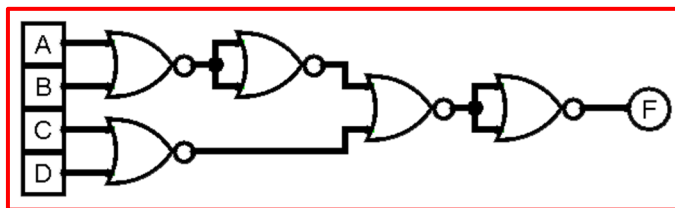

$X = A\overline{B}$ [0.5 pt]
$Y = \overline{XC}$ [0.5 pt]
$Z = \overline{B + C}$ [0.5 pt]
$F = Y + Z$ [0.5 pt]

(B)   Find a minimal implementation of the function below using only **2-input NOR gates**. [6 pts]

$$F = \overline{\overline{A}\,\overline{B}(C + D)}$$

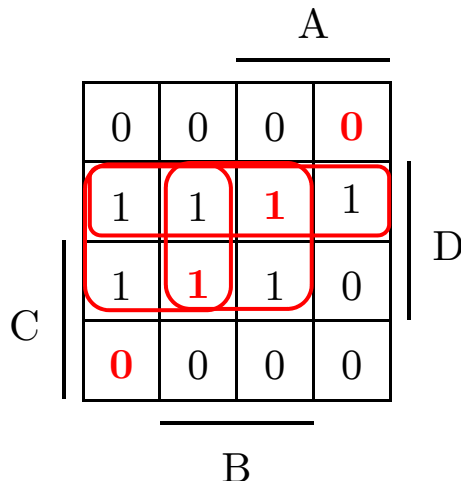
[2 pt] Valid gate conversion from expression
[2 pt] DeMorgan's applications (either in expression or gate)
[2 pt] Conversion of extra NOTs to NORs

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

$\mathbf{\overline{C}D + \overline{A}D + BD}$
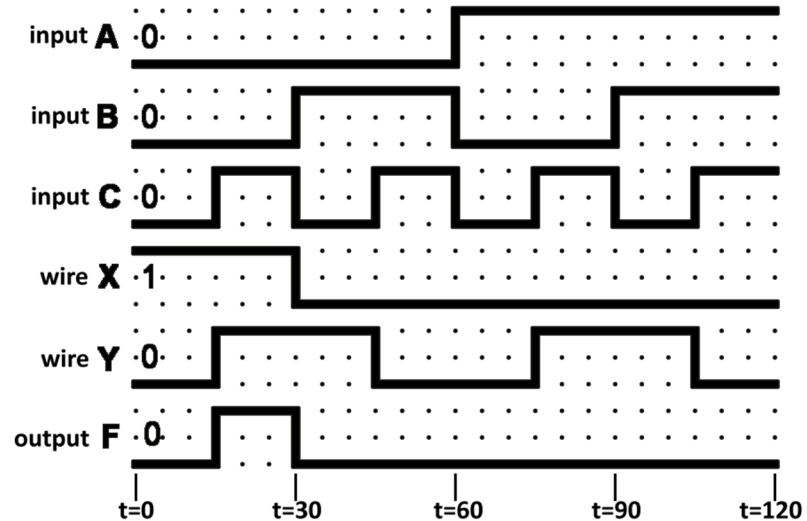
[2 pt] X choices: 0, 1, 1, 0
[1 pt each] correct term/grouping
[-0.5 pt each] smaller grouping used

Question 3: Waveforms & Verilog [11 pts]

For both parts below, consider the following desired truth table and the Verilog simulated testbench waveforms shown below.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(A)   Identify the time interval(s) where the testbench output does not match the desired functionality. Each horizontal tick represents 5 time units. [3 pts]
Incorrect in **[75,90] and [105,120]** (0 when it should be 1) [1.5 pt each].
[-0.5 pt each] if input combinations instead of time intervals.

(B)   If we know that X and Y are outputs of 2-input logic gates, complete the module Mystery below based on the testbench output. [8 pts]

```
module Mystery (F, A, B, C);
    output F;
    input  A, B, C;
    wire   X, Y;

    nor G1 (X, A, B); or assign X = ~(A|B);

    xor G2 (Y, B, C); or assign Y = B^C;

    and G3 (F, X, Y);
endmodule
```

[2 pt each] Correct input signals (A, B for X; B, C for Y)
[1 pt each] Correct gate (NOR for X, XOR for Y)
[1 pt each] Correct syntax (module names, argument order, assign keyword)