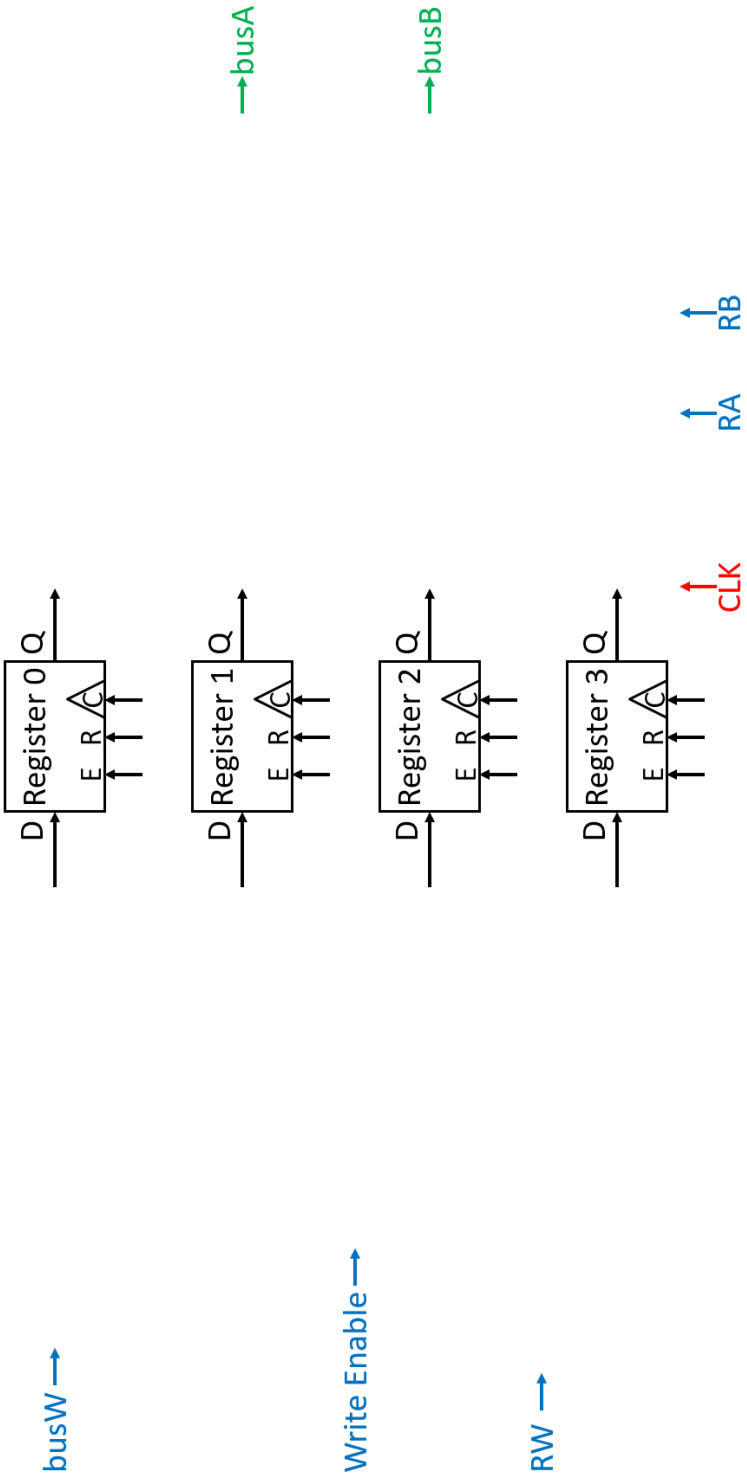
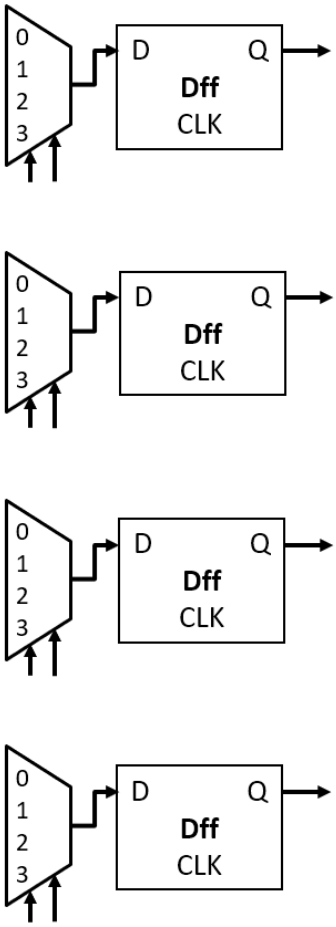
Register File

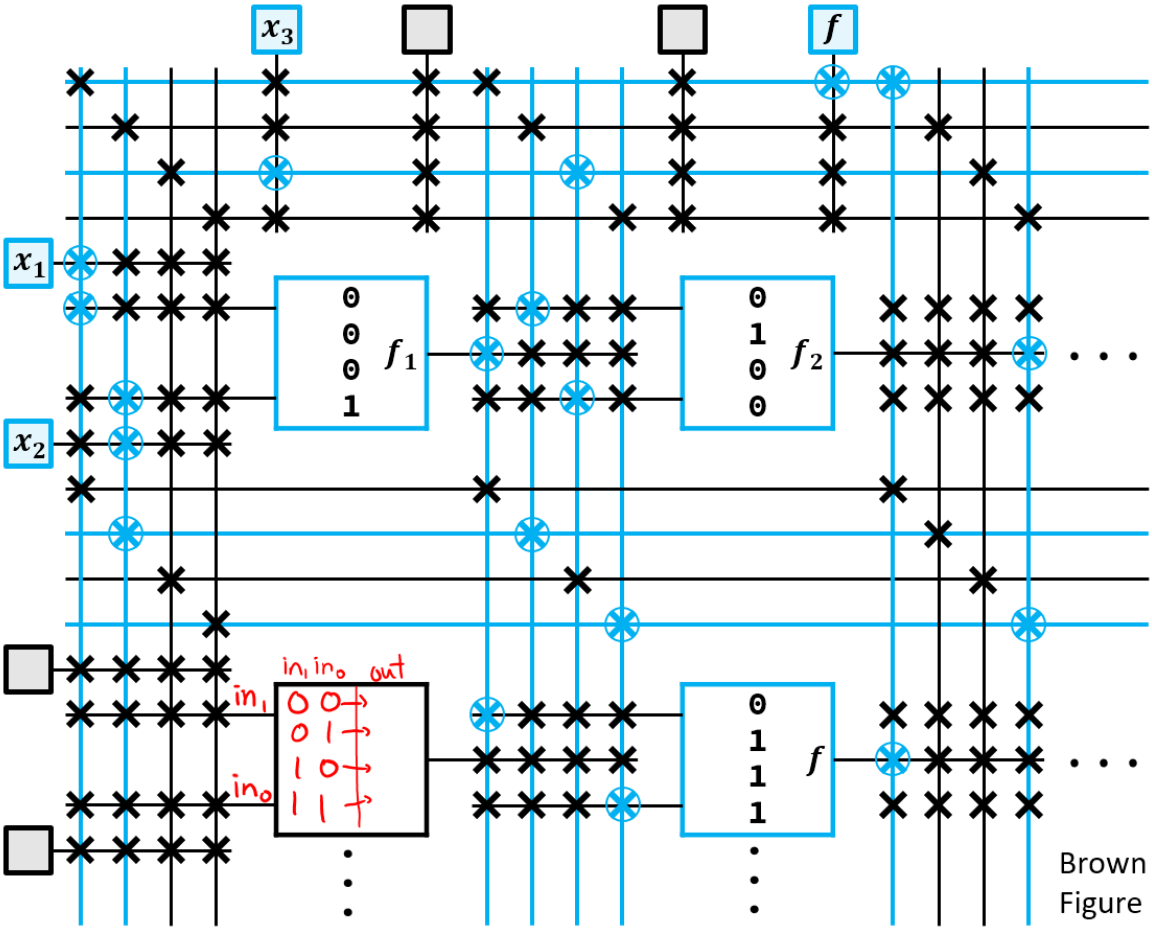


Shift Register



FPGA Routing

(Quartus says 🤖: HAHA LOSER NOW IT'S YOUR TURN)



Brown & Vranesic
Figure B.39

⊗ Connected ✕ Not connected